INTERNATIONAL DATA SCIENCES, INC.

ADVANCED TECHNIQUES IN DATA COMMUNICATIONS

MANUAL OF OPERATION

MODELS 1300 AND 1310

TDM-MODEM TEST SETS

MODEL 1300

MODEL 1310

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7 WELLINGTON ROAD, LINCOLN, R. I. 02865, TEL. 401-333-6200 TWX(710) 384-1911

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SYNOPSIS

Generates start-stop characters containing pseudo-random, alternate, mark or space data - Generates 5, 6, 7, 8 level characters with odd, even, or no parity and 1, 1.4, or 2 stop bits - Tests synchronous and asynchronous modems, and TDM and FDM multiplexer systems - Calculates and directly displays bit, character, or block error rates - Single or repeated blocks of bits or characters analyzed for error rate - Detects and tallies mark to space transitions - Eight LEDs monitor key signals at DTE or DCE interface - Full duplex....contains both a generator and an analyzer - Selected bit rate testing of asynchronous systems from 75 to 9600 bits/sec; synchronous systems up to 200,000 bits/sec - Bias distortion meter accurate to 1% - Complete self-test capability - Printer output capability.

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1.0 INTRODUCTION

The International Data Sciences TDM-Modem Test Set is a portable, completely self-contained unit capable of testing and analyzing any digital data transmission system. The test set may be used to test synchronous, asynchronous, or start-stop character-oriented systems such as time division multiplexers and character-oriented modems. Bit, character, and block error rates may be determined easily and accurately at the push of a button. The test patterns utilized are statistically optimum and accurately simulate computer generated data.

The test set contains both a data transmitter and data receiver. At the transmitter six data patterns may be generated either continuously or in a character format. These patterns are 63, 511, or 2047-bit pseudo-random sequences; alternate mark-space; steady mark; and steady space. Continuous characters may also be generated containing a start bit; 5, 6, 7, or 8 data bits; even, odd, or no parity bit; and 1, 1.4, or 2 stop bits. Any one of the six data patterns listed above may be selected as the data portion of the generated characters. Special repeating character sequences such as *, U (7-level ASCII), or R, Y (5-level Baudot) can also be generated.

1.1 Comprehensive Analysis Capability

The receiver section generates a true replica of the transmitted data and compares this replica with the received data. Bit errors, character errors, and block errors are thus detected and tallied. Simultaneously the total number of bits, characters, or blocks is also counted. Thus, the bit, character, or block error rate is continually computed and available at the touch of a button. The ability to perform an analysis on a single block (Model 1310 only) or continuous blocks of bits or characters is provided. Blocks of bits or characters from 10^3 (Model 1300) through 10^8 (Model 1310) may be selected for analysis. Error analysis is performed on data patterns and character sequences. In addition, a steady all-mark received pattern is analyzed for mark-to-space transitions which are detected, tabulated, and displayed. A bias meter continually monitors the received data signal and enables the operator to determine average mark or space bias to within 1% accuracy. Eight LED (light emitting diode) indicators and two switches allow the key signals in the DTE or DCE EIA interface to be continually monitored or controlled. Since the test set has both a transmitter and a receiver, tests may be performed on either an end-to-end or a loopback configuration. Figure 1.1 illustrates the use of the test set in a typical data network.

1.1 Comprehensive Analysis Capability (continued)

When externally timed for synchronous applications, the test set can operate at data rates up to 200,000 bits/sec. (See Section 4.2 for exceptions). For asynchronous application, internal timing is provided utilizing a high stability, crystal-controlled oscillator providing selection of the commonly used data rates of 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 bits/sec. The receiver contains a phase locked loop clock recovery circuit which is utilized to generate bit timing when testing asynchronous systems with continuous data. A character receiver is utilized when pseudo-random data characters framed with start and stop bits are being used to test an asynchronous system. In all cases, circuitry is provided to detect loss of synchronization and to automatically resynchronize the receiver. A comprehensive self-test capability is provided to enable the operator to completely test both the test set and the system all without disconnecting the test set from the multiplexer or modem. Separate connectors for DCE or DTE connections are provided on the back panel. An auxilliary option connector is provided on the rear panel allowing access to all key signals in the test set. The IDS Model 2000 Digital Printer also may be plugged into this connector to provide a permanent record of test results. A large selection of optional interfaces are available.

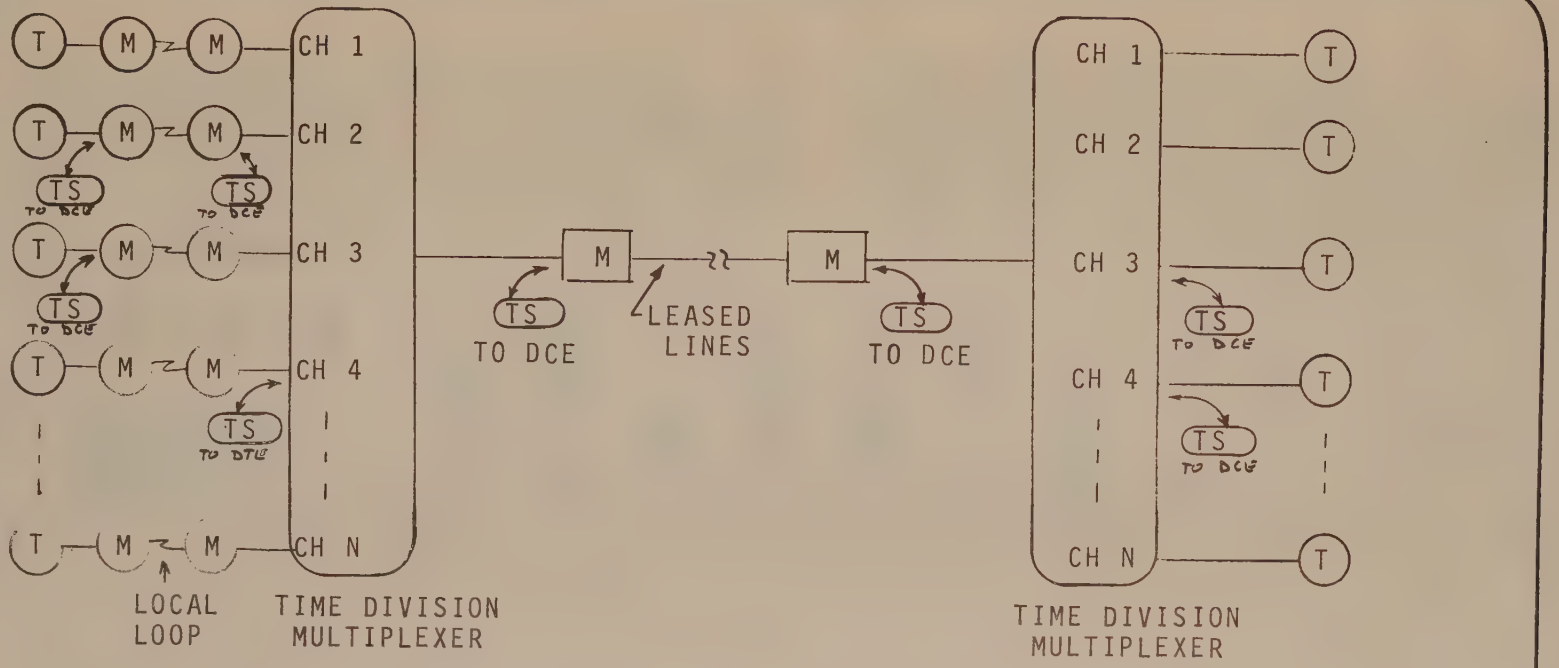
The front panel switches are grouped to perform specific functions. Figures 1.1-1 and 1.1-2 are pictorializations of the front and rear panels of the Models 1300 and 1310, respectively.

The Pattern switch selects the data pattern to be generated and analyzed for testing. An Invert Data toggle switch (Model 1300 only) is provided to invert both transmitted and received signals.

The Code Level, Stop Bits, and Parity switches allow control of the character format when it is desired to test systems utilizing pseudo-random data patterns grouped in a character format.

The Block Size (Model 1310 only), Bit/Char rotary switch, the Blocks Analyzed pushbutton, the Block Error-Bit Error Toggle switch, the Single-Continuous toggle switch (Model 1310 only), indicator (Model 1310 only) all allow the operator flexibility to perform comprehensive tests at the receiver to determine bit, block, and character error rates.

The Data Rate rotary switch allows the operator to perform synchronous testing at the modem rate or asynchronous testing at any one of the commonly used data rates. The Sync/Async toggle switch allows synchronous and asynchronous testing of internally and externally timed modems.



T = DATA TERMINAL EQUIPMENT

M = HIGH SPEED SYNCHRONOUS MODEMS

M = LOW SPEED ASYNCHRONOUS MODEMS

TS = MODEL 1300 OR 1310 TDM-MODEM TEST SET

FIGURE 1.1 The above diagram shows a typical data communication system containing both asynchronous and synchronous modems and time division multiplexers. Various tests which may be performed utilizing Model 1300 or 1310 TDM-Modem Test sets are indicated on channels 2, 3, and 4 and the high speed portion of the link. Note that since test sets have full duplex capability, tests may be performed using only a single test set simply by looping the remote modem or multiplexer.

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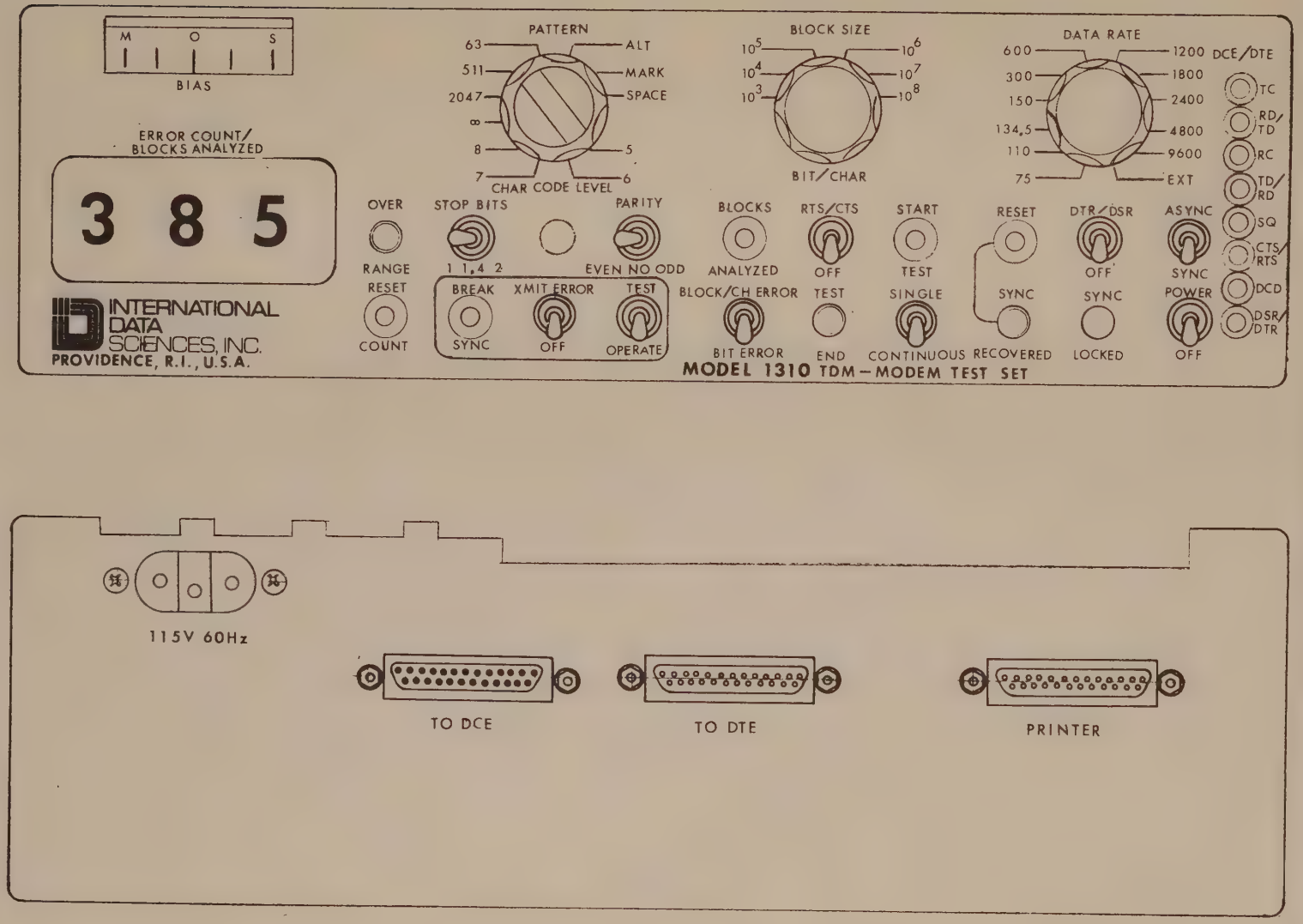

FIGURE 1.1-1 Front and Rear Panel Pictorialization of Model 1310

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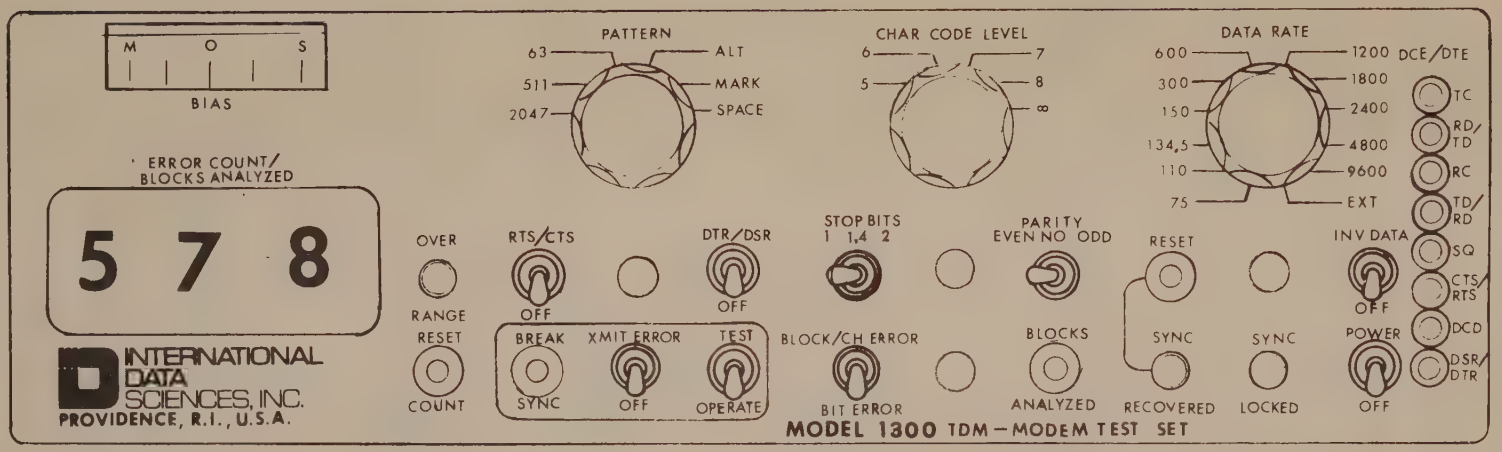

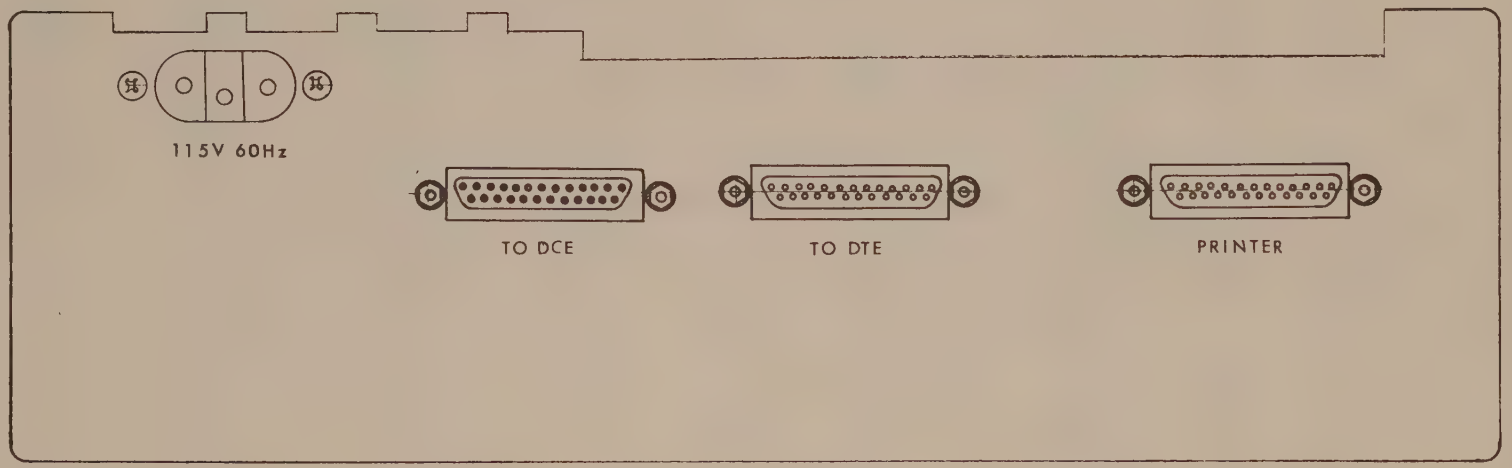

FIGURE 1.1-2 Front and Rear Panel Pictorialization of Model 1300.

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1.1 Comprehensive Analysis Capability (continued)

Eight LEDs monitor eight key signals in the EIA interface. In addition, two toggle switches enable the RTS (Request to Send) and the DTR (Data Terminal Ready) signals to be manually controlled.

The receiver synchronization functions are monitored by the Sync Locked and Sync Recovered indicator lamps along with the Reset pushbutton for the Sync Recovered lamp which has memory.

A three-digit display labeled Error Count/Blocks Analyzed with an Overrange indicator provides bit, block, character, or mark-to-space error counts and the total bit or character block counts. A Reset Count pushbutton allows the operator to reset all error and block counts.

A Bias meter analyzes all received data for average mark or space bias distortion.

Self-test of the units and the system under test is possible by means of the Break Sync pushbutton, the Xmit Error toggle switch, and the Test-Operate toggle switch.

And finally, the unit is powered and initialized by the Power switch.

1.2 Safety Precautions

Care should be taken when servicing the test set with the top cover removed. The AC line voltage has been insulated to prevent accidental shock.

1.3 Troubleshooting

A test procedure has been included in this manual for troubleshooting assistance. Each test is used to exercise a specific function and can be correlated with the schematics and parts lists for repair purposes.

1.4 Inspection

There are no moving parts in the test set. The unit can remain in service with only routine inspection while in service to insure proper operation.

1.5 Performance Verification

A test procedure has been included in this manual to be used to verify proper operation. See Section 7.0.

2.0 CONSOLE CONTROLS

The following console controls are located on the front panel of the test set. Each control is listed by its label. CAUTION: For reliable operation, the test set should be reset by turning power off and then on each time a control setting is changed.

2.1 Pattern

A six-position rotary switch with settings at 2047, 511, 63, Alt, Mark, and Space. This switch enables the operator to select any one of six different patterns to be used as data during the test. The 2047, 511, and 63 settings select pseudo-random sequences which repeat every 2047, 511, and 63 bits, respectively. The Alt, Mark, and Space settings select an alternate one-zero pattern, a steady mark or a steady space, respectively. The Baudot 5-level, R, Y pattern or the ASCII 7-level *, U can be generated by setting the Pattern switch to ALT and the Code Level switch to 5 or 7, respectively. Error analysis is performed on the 2047, 511, 63, and Alt patterns. Mark-to-Space transitions are counted on the Mark pattern.

2.2 Invert Data (Model 1300 only)

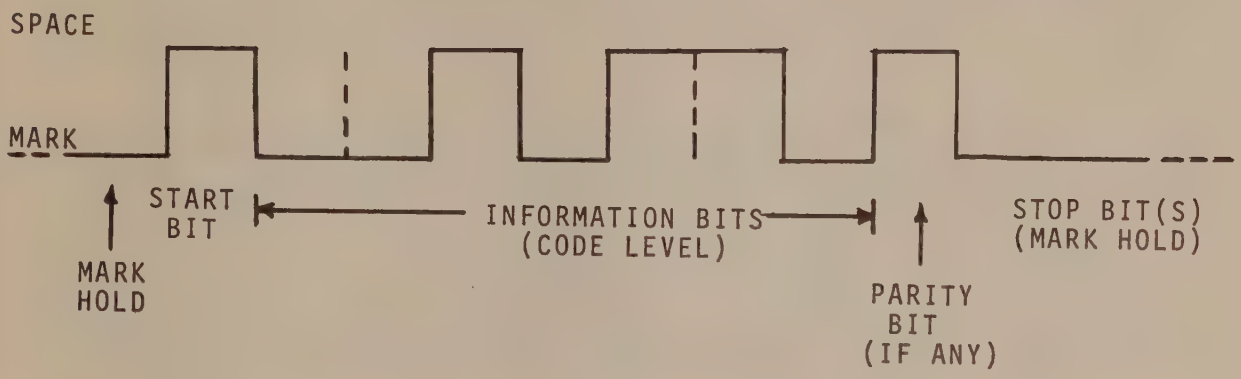
A two-position toggle switch labeled Inv. Data and Off. When in the Inv. Data position, all transmitted and received patterns, not including Start-Stop characters, are inverted. The Off position is for normal operation.

2.3 Code Level

A five-position rotary switch with settings at 5, 6, 7, 8, and Infinite bits. This switch determines how many bit positions in each character are allotted to data. The data contents of each character are determined by the setting of the pattern switch.

When this rotary switch is set to the position labeled Infinity, the test set performs its analysis on continuous serial data sequences composed entirely of data selected by the rotary switch labeled Pattern. At the receiver, with the switch in the Infinity position, a bit or block error analysis is performed on the 63, 511, and 2047-bit pseudo-noise patterns, and on the Alternate pattern. The receiver counts mark-to-space transitions on the Mark pattern. No analysis is performed on the Space pattern. Figure 2.3 illustrates the character configuration.

When this rotary switch is set to either the 5, 6, 7, or 8 level positions, all data, as selected by the Pattern switch, is generated in a character format as follows:



NOTE: MARK EQUALS A NEGATIVE VOLTAGE.
SPACE EQUALS A POSITIVE VOLTAGE.

FIGURE 2.3 ILLUSTRATION OF A TYPICAL CHARACTER

2.3 Code Level (continued)

A start bit followed by 5, 6, 7, or 8 data bits (as selected by the Code Level switch); followed by an even, odd, or no parity bit (as selected by the Parity switch); followed by a stop bit of 1, 1.4, or 2 bits duration (as selected by the three-position toggle switch labeled Stop Bits). The characters thus formatted are generated serially and continuously one after another. Note: With this switch set to any of these positions, if the pattern switch is set to the Mark position; then all Mark-to-Space transitions will be counted.

At the receiver, error analysis is performed on the data portion of each character when the Pattern switch is set to 63, 511, or 2047. Error analysis is also performed on the Baudot R, Y pattern (Pattern switch set to ALT and Code Level switch set to 5), and the ASCII *, U pattern (Pattern switch set to Alt and Code Level switch set to 7). Mark-to-Space transitions on the Mark pattern are counted. No analysis is performed on the Space pattern. The start and stop bits of each character are utilized for character framing and timing; thus, the operation of a terminal is accurately simulated.

Figure 2.3 illustrates the configuration of a typical character.

2.4 Stop Bits

A three-position toggle switch with settings at 1, 1.4, and 2. This switch selects the duration of the stop bit, in bit increments, that follow the data and parity contents of each character transmitted. (See Figure 2.3). This switch setting has no effect on the receiver since the receiver will accept any character with a stop bit of 1 or more bits in duration.

2.5 Parity

A three-position toggle switch with settings at Even, No, and Odd. When this switch is set to Even or Odd, an even or odd parity bit, respectively, will be assigned based upon the data contents of each character. This parity bit follows the data portion of each character. When this switch is set to the No position, the parity bit is eliminated and the data contents is followed by the stop bit(s) in each character as selected by the Stop Bits switch. (See Figure 2.3).

When the receiver is performing a mark-to-space transition analysis on a received all-mark signal, the data rate switch must be set to some position other than EXT.

2.5 Parity (continued)

At the receiver, no error analysis on parity is performed. Instead, a more complete error analysis on the entire character is done. The parity bit is utilized only to complete the character format and thus allow data communication systems containing character sensitive time division multiplexers and demultiplexers and certain character sensitive modems to be tested.

2.6 Data Rate

A twelve-position rotary switch with positions at 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 bits/sec data rates. These positions are used when interfacing with asynchronous modems or for selecting a transmitter clock to drive an externally timed synchronous modem. The position labeled EXT is used when interfacing with synchronous modems at speeds up to 200,000 bits/sec.

During self-test when the Test-Operate switch is set to test, the Data Rate switch is used to select a test data rate.

When the receiver is performing a mark-to-space transition analysis on a received all-mark signal, the data rate switch should be set to a position equal to twice or more the expected mark-to-space transition rate.

2.7 Block Size (Model 1310 only)

A six-position rotary switch labeled Block Size, Bit/Character with settings at 10^3, 10^4, 10^5, 10^6, 10^7, and 10^8. By means of this switch the operator is able to partition the received data into blocks of bits or blocks of characters depending on the setting of the Code Level rotary switch. If the Code Level switch is set to Infinity and the Pattern switch is set to any pattern except Space, then the Block Size is measured in bits. If the Code Level switch is set to 5, 6, 7, or 8, then the Block Size is measured in characters for all settings of the Pattern switch.

The Block Size switch is available on the Model 1310 only. On the Model 1300, the block size is internally strapped to 10^3 bits or characters.

2.8 Blocks Analyzed

A pushbutton switch which, when depressed, displays a three digit plus overrange count of the total number of blocks of either bits or characters that have been analyzed since the Reset Count pushbutton was last pushed. Thus, by means of this pushbutton,

2.8 Blocks Analyzed (continued)

the bit error rate, block error rate, or character error rate may be determined. All error analysis and bit, block, or character counting ceases while this pushbutton is depressed. Depressing and releasing this pushbutton will add one to the error count during Mark-to-Space transition analysis.

2.9 Block Error-Bit Error

A two-position toggle switch labeled Block Error-Bit Error which allows the operator to perform an error analysis on a bit, character, or block basis. If this switch is set to the Bit position, then all received data will be tested on a bit-by-bit basis for bit errors and the three-digit digital display will be increased by one each time a bit in error has been detected.

If this switch is set to Block Error position, the Code Level switch is set to the Infinity position, and the Pattern switch set to any position except Mark or Space, then the received data will be compared on a block-by-block basis where the block size in bits is determined by the setting of the Block Size rotary switch, and the digital error count display is increased by one each time a block of received data contains one or more errors.

If, on the other hand, this switch is set to Block Error and the Code Level switch is set to 5, 6, 7, or 8, then the received data is compared on a character-by-character basis where the block size in characters is determined by the setting of the Block Size rotary switch and the digital error count display is increased by one each time one or more data errors has been detected in a block of characters.

The error counts thus obtained, in conjunction with the total bit, block, or characters analyzed as provided by the Blocks Analyzed pushbutton, directly provide a continuous calculation of the bit, block, or character error rate.

2.10 Single-Continuous (Model 1310 only)

A two-position switch labeled Single and Continuous which enables the operator to perform tests either continuously or on a single block of data only. The size of the block is determined by the setting of the Block Size switch.

In the Single position, the error analysis on either a single block of bits or a single block of characters is performed depending on the setting of the Code Level switch. The error analysis is started by pushing the Start Test pushbutton switch. The Test End indicator will be illuminated when the block of bits or characters has been tested.

2.10 Single-Continuous (Model 1310 only) (continued)

In the Continuous position, data is analyzed as it is received bit-by-bit, character-by-character, or block-by-block depending upon the settings of the Code Level switch and the Bit Error-Block Error switch. If this switch is thrown from Continuous to Single, the test will end after the analysis of the current block is completed. The Test End indicator will illuminate to indicate when this occurs.

This switch is available only on the Model 1310. On the Model 1300, this switch is internally strapped to Continuous.

2.11 Start Test (Model 1310 only)

This pushbutton is active only when the Single-Continuous switch is in the Single position. Depressing this pushbutton starts the analysis of a single block of data either on a bit-by-bit or character-by-character basis depending on the setting of the Code Level switch.

This switch is available only on the Model 1310. The Model 1300 does not have the capability to run a test on a single block of data, only on continuous blocks of 10^3 bits or characters each.

2.12 Test End (Model 1310 only)

This indicator is illuminated when the analysis of a single block of received data, either bits or characters, depending on the setting of the Code Level switch, has been completed. This lamp operates only when the Single-Continuous switch is in the Single position. The lamp automatically is extinguished and testing resumes whenever the Start Test pushbutton is depressed. This lamp is turned on if power is applied to the test set with the Single-Continuous switch in the Single position.

The Test End lamp and its function are available only on the Model 1310.

2.13 Signal Monitoring

Ten key signals in the EIA interface are monitored by means of eight LEDs located on the front panel. The labeling of these eight LEDs are keyed according to whether the test set is plugged into a DCE or a DTE (DCE/DTE). These eight LEDs are labeled: TC (Transmit Clock); RD/TD (Received Data/Transmitted Data); RC (Received Clock); TD/RD (Transmitted Data/Received Data); SQ (Signal Quality); CTS/RTS (Clear to Send/Request to Send); DCE (Data Carrier Detect); DSR/DTR (Data Set Ready/Data Terminal Ready). All LEDs may be tested by depressing the Reset Count pushbutton.

2.13 Signal Monitoring (continued)

The TD, RD, TC, and RC indicators light only while transitions in the binary signal are detected. Figure 2.13 shows the signal flow between the front-panel LED monitors and the rear-panel connectors labeled To DCE and To DTE.

2.14 RTS/CTS (Model 1310 only)

This toggle switch allows the operator to control the Request to Send line in the "To DCE" interface or the Clear to Send line in the "To DTE" interface. When in the "OFF" position, transmitted data is held in the MARK position (MARK HOLD), i.e. the test set is only transmitting data when the RTS switch is set to ON.

2.15 DTR/DSR

This toggle switch allows the operator to control the Data Terminal Ready signal in the "To DCE" interface or the Data Set Ready signal in the "To DTE" interface.

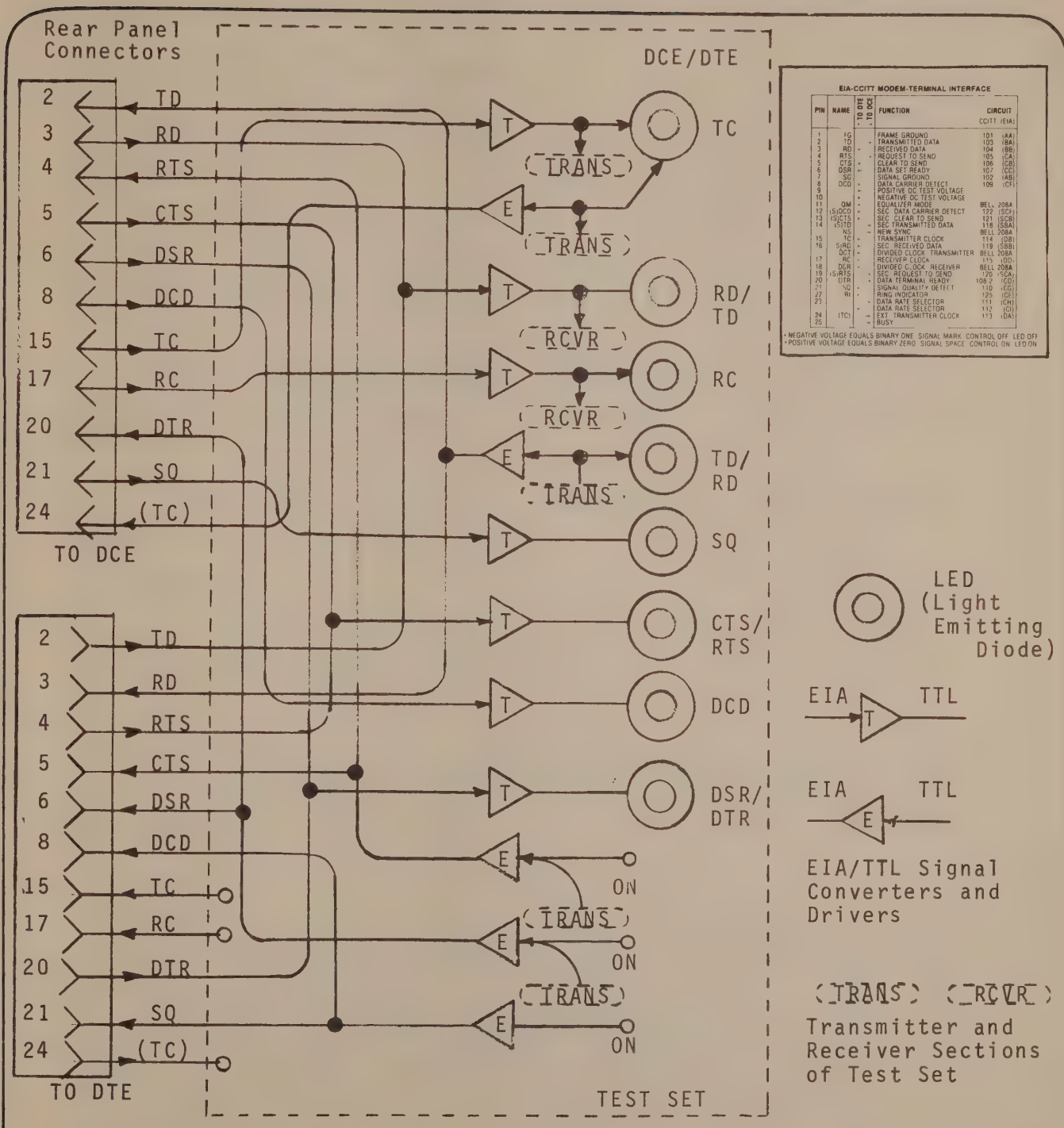
2.16 Sync Locked

This indicator is illuminated whenever the analyzer section of the test set is generating a pattern in phase with the pattern received on the received data line. Bit, character, or block error and mark-to-space transition detection is performed only when this light is illuminated.

2.17 Sync Recovered

This lamp when illuminated, indicates that the receiver had detected a loss of synchronization during the test and had automatically resynchronized and continued the error analysis. Once lit, the indicator remains on until extinguished by the Reset Sync Recovered pushbutton. Once lit, this lamp will turn off when the Sync Locked lamp turns off, but will turn on again when the Sync Locked lamp turns on.

When the Code Level switch is set to Infinity, the digital error count display is reset to zero each time a loss of synchronization is detected. When the Code Level switch is set to either the 5, 6, 7, or 8 position, the digital error count display is not reset to zero each time a loss of synchronization is detected.



EIA-CCITT MODEM-TERMINAL INTERFACE

PIN	NAME	TO DTE / TO DCE	FUNCTION	CIRCUIT CCITT (EIA)
1	FG	-	FRAME GROUND	101 (AA)
2	TD	→	TRANSMITTED DATA	103 (BA)
3	RD	←	RECEIVED DATA	104 (BB)
4	RTS	→	REQUEST TO SEND	105 (CA)
5	CTS	←	CLEAR TO SEND	106 (CB)
6	DSR	←	DATA SET READY	107 (CC)
7	SG	-	SIGNAL GROUND	102 (AB)
8	DCD	←	DATA CARRIER DETECT	109 (CF)
9		←	POSITIVE DC TEST VOLTAGE	
10		←	NEGATIVE DC TEST VOLTAGE	
11	QM	-	EQUALIZER MODE	BELL 208A
12	(SI)DCD	←	SEC. DATA CARRIER DETECT	122 (SCF)
13	(SI)CTS	←	SEC. CLEAR TO SEND	121 (SCB)
14	(STD)	→	SEC. TRANSMITTED DATA	118 (SBA)
	NS	→	NEW SYNC	BELL 208A
15	TC	←	TRANSMITTER CLOCK	114 (DB)
16	SRD	←	SEC. RECEIVED DATA	119 (SBB)
	DCT	←	DIVIDED CLOCK TRANSMITTER	BELL 208A
17	RC	←	RECEIVER CLOCK	115 (DD)
18	DCR	←	DIVIDED CLOCK RECEIVER	BELL 208A
19	(SI)RTS	→	SEC. REQUEST TO SEND	120 (SCA)
20	DTR	→	DATA TERMINAL READY	108.2 (CD)
21	SQ	←	SIGNAL QUALITY DETECT	110 (CG)
22	RI	←	RING INDICATOR	125 (CE)
23		→	DATA RATE SELECTOR	111 (CH)
		←	DATA RATE SELECTOR	112 (CI)
24	(TC)	→	EXT. TRANSMITTER CLOCK	113 (DA)
25		←	BUSY	

• NEGATIVE VOLTAGE EQUALS BINARY ONE SIGNAL MARK CONTROL OFF LED OFF
• POSITIVE VOLTAGE EQUALS BINARY ZERO SIGNAL SPACE CONTROL ON LED ON

FIGURE 2.13 SIGNAL FLOW DIAGRAM BETWEEN FRONT-PANEL LED MONITORS AND REAR PANEL CONNECTORS LABELLED TO DCE AND TO DTE.

2.18 Error Count/Blocks Analyzed

When the Block Error-Bit Error switch is set to Bit Error, this three-digit decimal display provides a direct readout of the accumulated bits in error that have been detected. When the Block Error-Bit Error switch is in the Block Error position, this display provides a direct readout of the accumulated number of characters or data blocks that have been received in error. When the Pattern switch is set to the Mark position, this Display provides a direct readout of the accumulated number of mark-to-space transitions that have occurred.

When the pushbutton labeled Blocks Analyzed is depressed, the decimal display provides a direct readout of the number of blocks of bits or blocks of characters that have been analyzed, depending upon whether the Code Level switch is or is not, respectively, set to Infinity.

The Error Count, Blocks Analyzed count and their overrange indicators are all reset to zero by means of the Reset Count pushbutton.

2.19 Overrange

This indicator is illuminated each time the quantity being displayed by the decimal display exceeds 999. This indicator is reset by the Reset Count pushbutton.

2.20 Reset Count

This pushbutton resets the error counter, the block counter, and their respective overrange indicators. The eight monitor LEDs are also illuminated each time this pushbutton is depressed as an LED test.

2.21 Bias

This meter constantly monitors the signal appearing on the Received Data line and measures the mark or space bias distortion. The meter is calibrated in percent and labeled M at the left end indicating 100% distortion in the mark direction; S at the right end indicating 100% distortion in the space direction; and 0 at the center indicating no distortion. Intermittent markings are at the 10% increments. The meter is capable of measuring distortion in 1% increments.

2.22 Xmit Error

A toggle switch that causes the insertion of one error per pseudo-noise sequence to be transmitted. Detection of the error

2.22 Xmit Error (continued)

at the receiver provides a positive indication that data transfer and error analysis is occurring. No errors are inserted in the Alt, Mark, or Space patterns.

2.23 Test-Operate

In the Test position, the transmitted data is directed to the receiver input terminal. Self-test of the transmitter and the receiver then takes place at a rate determined by the Data Rate selector switch. This mode will allow operation of the unit independent of external equipment to test its operation. In the Operate position, the unit is conditioned for normal operation. This switch operates in conjunction with the RTS switch. In order to self-test the test set, RTS must be set to ON (Model 1310 only).

2.24 Break Sync

This pushbutton causes the receiver to become non-synchronized with the Receive Data signal. Allows self-test of the sync loss detection and auto-resynchronization circuitry. When analyzing the Alt pattern, this pushbutton may have to be pushed several times before a loss of sync is initiated.

2.25 Power

The power switch energizes and automatically initializes the unit including its counters and sync status circuitry.

2.26 Sync/Async (Model 1310 only)

This two-position toggle switch allows the test set to operate with those synchronous modems which are externally timed at the transmitter. This switch must be set to the Sync position when testing synchronous modems both internally or externally times and set to the Async position when testing asynchronous modems.

When testing synchronous modems that supply transmit clock to the terminal, the Data Rate switch must be set to the EXT position and the Sync/Async switch set to the Sync position. When testing synchronous modems that require the terminal to supply transmitter clock, the Data Rate switch must be set to the channel data rate (whereby a timing clock at the selected data rate is applied to pin 24 of the EIA interface data connector labeled To DCE thus supplying the necessary external timing to the modem), and the Sync/Async switch set to the Sync position.

2.26 Sync/Async (Model 1310 only) (continued)

When testing asynchronous modems, the Sync/Async switch must be set to the Async position and the desired operating data rate selected by means of the Data Rate switch.

Table 2.26 lists the various combinations of Sync/Async switch and Data Rate switch settings and the resultant operations. Note that setting the Sync/Async switch to the Async position and the Data Rate switch to the ext (external) position is invalid and the test set will not function properly. Also, setting the Sync/Async switch to the Sync position and the Code Level switch to the NOT positions is also invalid and the test set will not function properly.

TABLE 2.26 SYNC/ASYNC, DATA RATE AND CODE LEVEL SWITCH SETTINGS.

SWITCH SETTINGS			
SYNC-ASYNC SWITCH	DATA RATE ROTARY SWITCH	CODE LEVEL ROTARY SWITCH	RESULTANT OPERATION OF TEST SET
ASYNC	NOT EXT	∞	Asynchronous operation. Data in continuous format.
ASYNC	NOT EXT	NOT ∞	Asynchronous operation. Data in start-stop character format.
SYNC	NOT EXT	∞	Synchronous operation. Data in continuous format. Transmit clock supplied to modem at rate selected by Data Rate rotary switch.
SYNC	EXT	∞	Synchronous operation. Data in continuous format. Modem supplies all timing.
ASYNC	EXT	∞ OR NOT ∞	Invalid combinations. Test Set inoperative.
SYNC	EXT OR NOT EXT	NOT ∞	

3.0 SPECIFICATIONS

3.1 Power

105 to 125 VAC, 60 Hz, or 210 to 250 VAC, 50 Hz (strapped at factory). Approximately 35 watts.
Fuse: 3/4 Amp, Slow Blow.

3.2 Operating Temperature

0°C to 50°C (32 F to 122 F)

3.3 Size

Desktop:	Width	12 1/4"	(31.75 cm)
	Height	4"	(10.16 cm)
	Depth	8 5/8"	(21.9 cm)

3.4 EIA RS-232 Interface

All signals conform to EIA RS-232/CCITT V.24 specifications. Two connectors labeled To DCE (Data Communication Equipment) and To DTE (Data Terminal Equipment) are mounted on the rear panel and are used to connect the test set to the data communication equipment and the data terminal equipment, respectively. The signals on each of these connectors are listed in Table 3.4. Figure 3.4 is a replica of the EIA interface decal which is affixed to the rear panel of each test set.

The input signals are Received Data, Transmitter Clock, and Receiver Clock, all required to be low-level and polar, suitable for use with electronic circuitry. In the test set, these signals are processed through double threshold hysteresis circuits to allow high noise immunity.

The standard test set with RS-232 interface has a noise immunity of four volts nominal. The negative threshold is set at minus two volts and the positive threshold is set at plus two volts. Clamping circuitry allows the positive threshold to be exceeded with signals as large as plus 25 volts and the negative threshold to be exceeded with signals as large as minus 25 volts. See Figure 3.4-1 and 3.4-2 for threshold and interrelationship details.

TABLE 3.4 "TO DCE" AND "TO DTE" CONNECTOR SIGNALS

TO DCE CONN. PIN	TO DTE CONN PIN	CCITT V.24 DESIGNATION	RS232B OR C DESIGNATION	TITLE	DESCRIPTION ON = POS. VOLT. = SPACE = BINARY 0 OFF = NEG. VOLT. = MARK = BINARY 1
1	1	101	AA	Protective Ground	This lead is an electrical equipment frame and power ground.
2	3	103	BA	Transmitted Data (TD)	This lead carries the signals that originate in the test set and are to be transmitted by the DCE or DTE to a distant station. An output from the test set.
3	2	104	BB	Received Data (RD)	This lead carries the signals that are generated by the DCE or DTE in response to signals from a distant station. An input to the test set.
4	5	105	CA	Request to Send (RTS)	An "on" condition on this lead indicates that the test set is ready to transmit data. An output from the test set.
5	4	106	CB	Clear to Send (CTS)	An "on" condition on the lead indicates that the DCE or DTE is ready to transmit data from the test set to a distant terminal. An input to the test set.
6	20	107	CC	Data Set Ready (DSR)	An "on" condition on this lead indicates that the DCE or DTE is ready to process data. An input to the test set.
7	7	102	AB	Signal Ground	This lead established the common ground reference potential for all circuits except protective ground.
8	Not Used	109	CF	Receive Line Signal (Data Carrier Detector) (DCD)	This lead provides an indication that data carrier signals from the remote station are being received by the DCE or DTE. An input to the test set.

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TABLE 3.4 "TO DCE" AND "TO DTE" CONNECTOR SIGNALS (continued)

TO DCE CONN. PIN	TO DTE CONN. PIN	CCITT V.24 DESIGNATION	RS232B OR C DESIGNATION	TITLE	DESCRIPTION ON = POS. VOLT = SPACE = BINARY 0 OFF = NEG. VOLT. = MARK BINARY 1
9-11	9-11	-	-	-	Not Used.
12	12	122	SCF	Secondary Receive Line Signal (Data Carrier) Detector (DCD) (s)	Not Used
13	13	121	SCB	Secondary Clear to Send (CTS)(s)	Not Used
14	14	118	SBA	Secondary Transmitted Data (TD)	Not Used
15		114	DB	Transmitted Signal Element Timing (TC)	Signals on this line are used to provide the test set with signal element timing information. An input to the test set. Not used when testing asynchronous DCE or DTE
16	16	119	SBB	Secondary Received Data (RD)(s)	Not Used
17		115	DD	Receiver Signal Element Timing (RC)	Signals on this line are used to provide the test set with the signal element timing information. An input to the test set. Not used when testing async. DCE or DTE.

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TABLE 3.4 "TO DCE" AND "TO DTE" CONNECTOR SIGNALS (continued)

TO DCE CONN. PIN	TO DTE CONN. PIN	CCITT V.24 DESIGNATION	RS232B OR C DESIGNATION	TITLE	DESCRIPTION ON = POS. VOLT. = SPACE = BINARY 0 OFF = NEG. VOLT. = MARK = BINARY 1
18	18	-	-	-	Not used
19	19	120	SCA	Secondary Request to Send (RTS)(s)	Not Used
20	6	108.2	CD	Data Terminal Ready (DTR)	An "on" condition on this lead indicates that the test set is ready to process data. An output from the test set.
21		110	CG	Signal Quality Detector (SQ)	An "on" condition on this lead indicates that signal quality received by the DCE is above a prescribed threshold. An input to the test set.
22	22	125	CE	Ring Indicator	Not used by test set.
23	23	111/112	CH/CI	Data Signal Rate Selector	Not used by test set.
24		113	DA	Transmitter Signal Element Timing	Signals on this line are used to provide the transmitting DCE with signal element timing information. An output from the test set selectable with the Sync/Async switch.
25	25	-	-	-	Not used.

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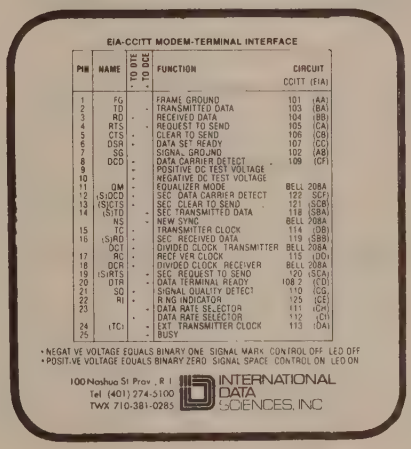

EIA-CCITT MODEM-TERMINAL INTERFACE

PIN	NAME	* TO DTE	* TO DCE	FUNCTION	CIRCUIT CCITT (EIA)
1	FG			FRAME GROUND	101 (AA)
2	TD		-	TRANSMITTED DATA	103 (BA)
3	RD	-		RECEIVED DATA	104 (BB)
4	RTS		-	REQUEST TO SEND	105 (CA)
5	CTS	-		CLEAR TO SEND	106 (CB)
6	DSR	-		DATA SET READY	107 (CC)
7	SG			SIGNAL GROUND	102 (AB)
8	DCD	-		DATA CARRIER DETECT	109 (CF)
9		-		POSITIVE DC TEST VOLTAGE	
10		-		NEGATIVE DC TEST VOLTAGE	
11	QM	-		EQUALIZER MODE	BELL 208A
12	(S)DCD	-		SEC DATA CARRIER DETECT	122 (SCF)
13	(S)CTS	-		SEC CLEAR TO SEND	121 (SCB)
14	(S)TD		-	SEC TRANSMITTED DATA	118 (SBA)
	NS		-	NEW SYNC	BELL 208A
15	TC	-		TRANSMITTER CLOCK	114 (DB)
16	(S)RD	-		SEC RECEIVED DATA	119 (SBB)
	DCT	-		DIVIDED CLOCK TRANSMITTER	BELL 208A
17	RC	-		RECEIVER CLOCK	115 (DD)
18	DCR	-		DIVIDED CLOCK RECEIVER	BELL 208A
19	(S)RTS		-	SEC REQUEST TO SEND	120 (SCA)
20	DTR		-	DATA TERMINAL READY	108.2 (CD)
21	SQ	-		SIGNAL QUALITY DETECT	110 (CG)
22	RI	-		RING INDICATOR	125 (CE)
23			-	DATA RATE SELECTOR	111 (CH)
		-		DATA RATE SELECTOR	112 (CI)
24	(TC)		-	EXT TRANSMITTER CLOCK	113 (DA)
25		-		BUSY	

*NEGATIVE VOLTAGE EQUALS BINARY ONE SIGNAL MARK CONTROL OFF LED OFF
*POSITIVE VOLTAGE EQUALS BINARY ZERO SIGNAL SPACE CONTROL ON LED ON

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FIGURE 3.4 EIA MODEM-TERMINAL INTERFACE DECAL.

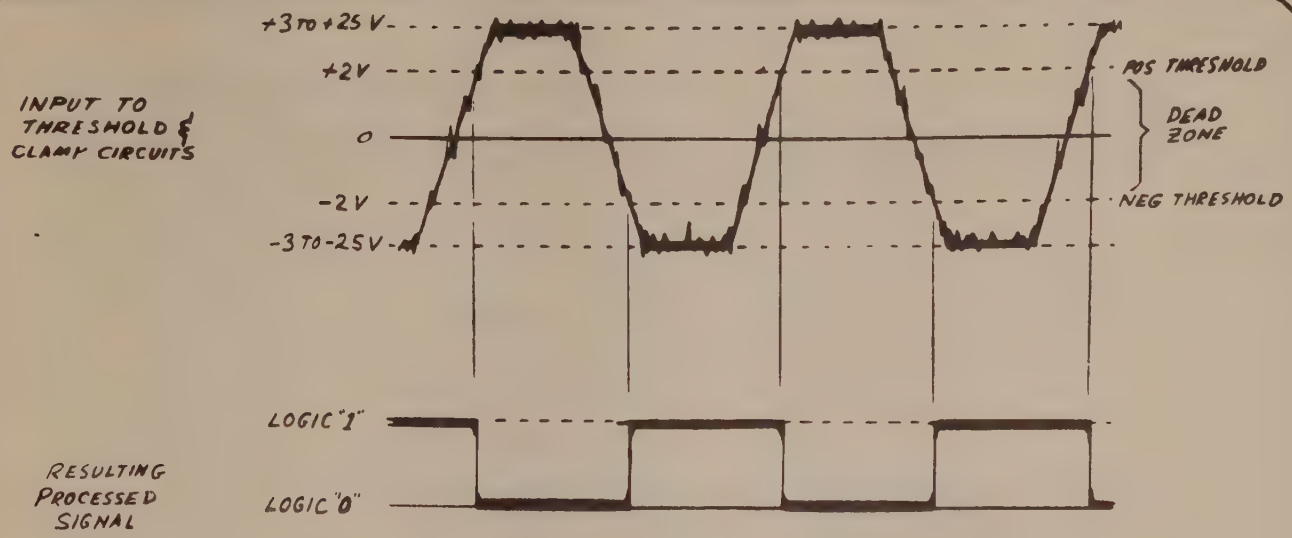
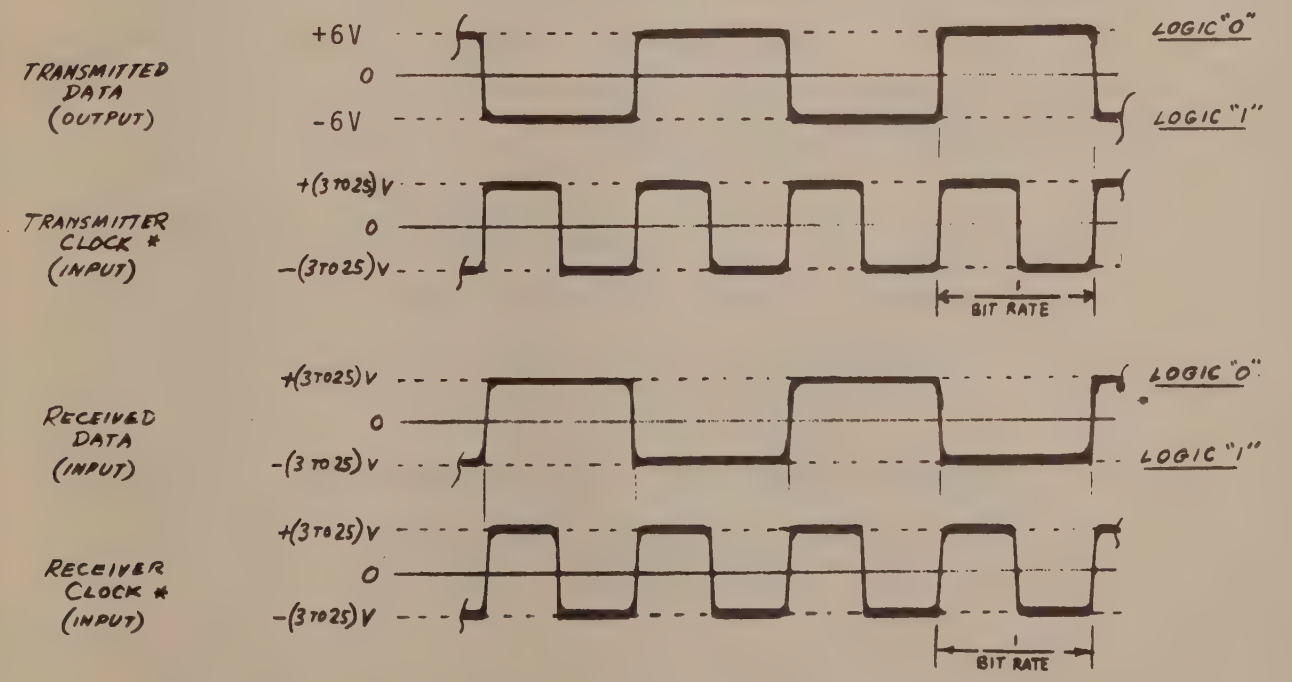


FIGURE 3.4-1 PROCESSING OF INPUT SIGNALS



* CLOCK SIGNALS REQUIRED IN SYNCHRONOUS APPLICATIONS ONLY.

FIGURE 3.4-2 CLOCK/DATA INTERRELATIONSHIPS

3.4 EIA RS-232 Interface (continued)

The EIA RS-232 Interface utilizes standard 25-conductor EIA cables with Cinch-Jones DB25S and DB25P connectors.

3.4.1 Interface Output Drivers

Levels - ±6V ±0.5 volts

Binary one - -6V ±0.5 volts

Binary zero - +6V ±0.5 volts

Impedance - Less than 100Ω for Data and clock signals. Less than 1000Ω for control signals.

Control Signals On, Space - +12V ±1 volt

Control Signals Off, Mark - -12V ±1 volt

Protection - All outputs protected against circuits to +25 volts, -25 volts, or ground

3.4.2 Interface Input Receivers

Binary one - -2 volts to -25 volts

Binary zero - +2 volts to +25 volts

Impedance - 3000Ω to 7000Ω

Noise Immunity - ±2 volts with hysteresis

Protection - ±25 volts without damage to receiver circuits

3.5 Printer (Option) Connector

An additional output connector labeled Printer (or Option on some units) is located on the rear panel to provide signals required for remote monitoring control, data recording, and more detailed test and analysis. The connector is a Cinch-Jones DB25S. It provides compatibility with the IDS Model 2000 Test Set Printer. All important signals are available at this connector and are listed in Table 3.5.

WARNING!! For proper operation of test set, the IDS Model 2000 Test Set Printer must be turned ON when plugged into the TDM-Modem Test Set Printer connector.

3.6 Power Conversion To 230 VAC, 50 Hz

The following changes are necessary in order to operate the test set at 230 VAC, 50 Hz. See Figure 3.6.

3.6.1
Remove the back panel by removing the four screws located on the rubber feet.

3.6.2
Locate the brown wire tied to the transformer. Cut this wire approximately one inch from the transformer. Insulate the end connected to the transformer. This end will remain unused. Connect the other end of the brown lead to the white lead of the transformer and insulate the connection.

3.6.3
Re-install the rear panel by screwing on the four rubber feet.

3.6.4
Change the label on the back panel to read "230 VAC, 50 Hz".

TABLE 3.5 OPTION CONNECTOR SIGNALS

ALL OUTPUT SIGNALS ARE EITHER +5 VOLTS OR 0 VOLTS UNLESS OTHERWISE INDICATED

PIN	SIGNAL	DESCRIPTION
15	1 Unit	BCD Error Counter Readout (0 volts = "One")
14	2 Units	"
12	4 Units	"
13	8 Units	"
10	1 Ten	"
11	2 Tens	"
8	4 Tens	"
9	8 Tens	"
6	1 Hundred	"
7	2 Hundred	"
5	4 Hundred	"
4	8 Hundred	"
17	Reset Error Counter	An external negative pulse resets Error Counter to zero and clears overflow indicator.
24	Receiver in Sync	Signal is 0 volts when receiver is in sync, +5 volts when out of sync.
19	Sync Recovered	Zero level indicates sync has been recovered.
16	Transmitter clock	Transmit timing.
22	Receiver clock	Modem clock if synchronous, recovered clock if asynchronous. For bit sync purposes.
1	Start of Trans. Period	Periodic pulse appearing at the beginning of each Pseudo-Random pattern transmitted.
23	Start of Receiver Period	Periodic pulse appearing in phase with the beginning of each Pseudo-Random pattern received.
3	Clock Monitor	Positive level indicates clock is present at receiver.
2	Error Pulse	A negative pulse appears each time an error is detected in received sequence.
18	Transmitter Data	Transmitted Pseudo-Random Sequence (±6 volts).
20	Received Data	Received Pseudo-Random Sequence (±6 volts).
21	Signal Ground	
25	Chassis Ground	

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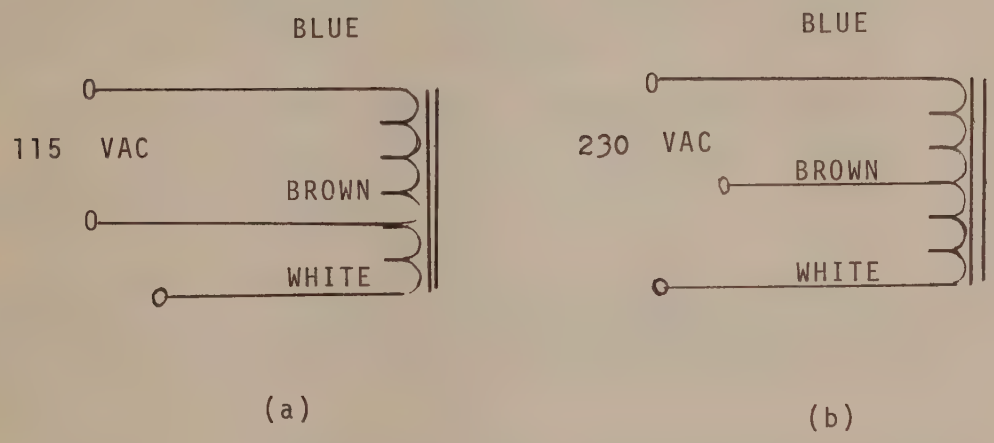


FIGURE 3.6 SCHEMATIC DIAGRAM FOR OPERATION AT (a) 115 VAC, 60 Hz AND (b) 230 VAC, 50 Hz.

4.0 INTERFACE OPTIONS

Four switch selectable interfaces, in addition to the standard EIA RS-232, are available as options on the Models 1300/1310. They are: Balanced V.35, Current (301/303), Mil 188, and TTL. The V.35, Current, and TTL interfaces are connected to the test set via separate 15 or 25-pin connectors. A special cable is associated with each interface.

Since the interfaces are switch selectable, all interface cables may be plugged into the test set at once since only the interface selected by the interface switch is activated. The interface selector switch is mounted on the rear panel.

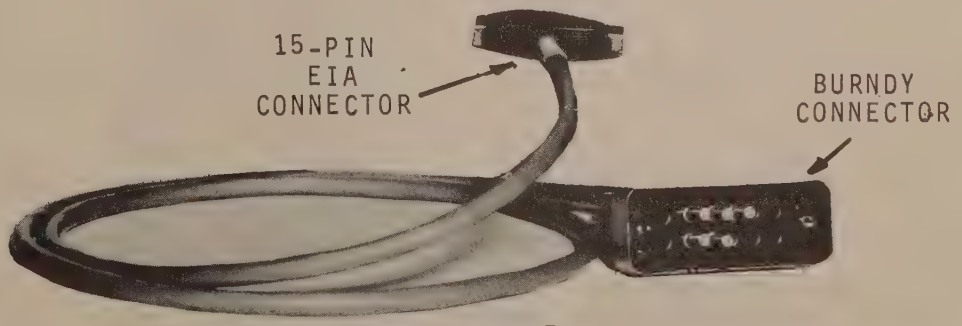
4.1 301/303 50 Kilobit Current Interface with Adaptor Cable Option

The Current Interface option for the Models 1300 and 1310 TDM-Modem Test Set consists of an additional connector mounted on the chassis rear panel.

A special cable is provided with this option and is shown in the photo below. This cable is equipped with a male, 15-pin connector at one end and a male Burndy connector at the other end. The pin assignments for the connectors and cables are given in Table 4.1.

The Current Interface option allows the test set to operate with all Bell 301/303 type wideband data sets at all speeds up to 230.4 kilobits/sec.

An internal clock of 50 KHz or 56 KHz is available as an option.



CURRENT INTERFACE CABLE

TABLE 4.1 CURRENT INTERFACE CABLE & CONNECTORS PIN ASSIGNMENTS

DTE (TEST SET) INTERFACE PIN #	IN/OUT	FUNCTION	DESCRIPTION	DCE INTERFACE PIN #
1	IN	Receive Data	Pseudo-Random Data, nonreturn-to-Zero.	K
2	IN	Serial Clock Receive	A current square wave clock used to time the sampling of the Received Data Signal.	L
3	IN	Serial Clock Transmit	A current square wave clock used to time the Transmit Data Signal.	J
4	OUT	Transmit Data	Pseudo-Random Data, nonreturn-to-Zero. Data changes on positive transitions of Transmit Clock Signal.	E
5	OUT	Request To Send	The binary zero state on this line conditions the modem to transmit.	D
6	-	Signal Ground	Provides reference for input and output signals. Except M&F.	Shields
7	OUT	Serial Clock Transmit External	Supplies a transmit clock to modem at 50 Kbps or 56 Kbps according to External timing option. (See Section 5.5)	H
8	IN	Data Set Ready	-	F
9	IN	Signal Quality	-	M
10	IN	Clear to Send	-	C
11-15			NOT USED	

NOTE: The connector which plugs into the Test Set is a Cynch Jones DB15P and the connector which plugs into the Modem is a Burndy MD12MXP-17TC.

4.1 301/303 50 Kilobit Current Interface with Adaptor Cable Option (continued)

A special 15 conductor cable with Cinch-Jones DB15P and Burndy MD12MXP-17TC connectors is used with this interface.

4.1.1 Interface Output Drivers

Binary one, Mark, Off - A current less than 5 ma into a 100Ω load.

Binary zero, Space, On - A current greater than 23 ma into a 100Ω load.

4.1.2 Interface Input Receivers

Binary one, Mark, Off - A current less than 5 ma

Binary zero, Space, On - A current greater than 23 ma

Impedance - 100Ω ±5%

Open circuit - Receiver assumes an off or mark-hold condition.

4.2 MIL 188/EIA RS-232 Interface (Switchable)

This interface is switch selectable with the EIA RS-232 interface and utilizes the same connectors and same cable. Thus, the connector pin assignments are the same as shown in Table 3.4.

When a MIL/EIA switchable interface is provided, capacitors are added to input circuits on the low threshold circuits. In this configuration, the operating speeds are as follows:

MIL: 200 KHz
EIA: 30 KHz

4.2.1 Interface Output Drivers

Levels - ±6V ±0.5 volts

Data Binary one - ±6V ±0.5 volts

Data Binary zero - -6V ±0.5 volts

Impedance - Less than 100Ω for data and clock signals. Less than 1000Ω for control signals.

4.2.1 Interface Output Drivers (continued)

Control Signal On, Space, Zero - +12V ±1 volt

Control Signal Off, Mark, One - -12V ±1 volt

Protection - All outputs protected against short circuits to -25 volts, +25 volts, or ground.

4.2.2 Interface Input Receivers

Data Binary one - +6 volts nominal

Data Binary zero - -6 volts nominal

Impedance - 6000Ω minimum

Noise Immunity - ±0.6 volts with hysteresis

Protection - ±25 volts without damage to receiver circuits.

4.3 Balanced CCITT V.35 Interface with Cables

This interface utilizes a special 25 conductor cable with Cinch-Jones and Continental connectors. All control signals conform to EIA RS-232 specifications. The pin assignment list is given in Table 4.3. An internal clock at 50 KHz or 56 KHz is available as an option.

4.3.1 Interface Output Drivers

Levels - ±1.1V +0.1 volt

Impedance - 100Ω ±1% balanced
150Ω ±1% with respect to ground
with outputs A and B shorted together

Binary One - Output A negative with respect to output B

Binary Zero - Output A positive with respect to output B

Rise and Fall Time - Greater than 40 nsec when measured between 10% to 90% of waveform rise or fall time.

TABLE 4.3

BALANCED CCITT V.35 INTERFACE CABLE (WHT/RED SLEEVING)

PIN ASSIGNMENT LIST

DTE (TEST SET) END INTERFACE PIN #	FUNCTION	DCE (MODEM) END INTERFACE PIN #
1	Protective Ground (EIA CKT AA)	A
2	Request to Send (EIA CKT CA)	C
3	Received Data (A)	R
4	Received Data (B)	T
5	Serial Clock Receive (A)	V
6	Serial Clock Receive (B)	X
7	Signal Ground (EIA CKT AB)	B
8	Not Used	
9	Serial Clock Transmit EXT (A)	U
10	Serial Clock Transmit EXT (B)	W
11	Serial Clock Transmit (A)	Y
12	Serial Clock Transmit (B)	A
13	Data Terminal Ready (EIA CKT CE)	H
14	Send Data (A)	P
15	Send Data (B)	S

NOTE: The connector which plugs into the Test Set is a Cinch Jones DB15S and the connector which plugs into the Modem is a Continental 25034-16PSKH-C.

4.3.1 Interface Output Drivers (continued)

DC Offset - 0V ±0.2 volts for each output with respect to ground

Protection - Outputs protected against short circuits to ground or to each other.

4.3.2 Interface Input Receivers

Sensitivity - ±10 millivolts maximum

Impedance - 100Ω ±1%

DC Resistance - 150Ω ±1% with respect to ground with inputs A and B shorted together

DC Offset - ±0.6 volts maximum

Protection - ±10 volts maximum without damage to receiver circuits

4.4 DTL or TTL/EIA RS-232 Interface (Switchable)

This interface is switch selectable with the EIA RS-232 interface. However, a separate 15-conductor cable is utilized for the DTL or TTL signals. The pin assignment listing is given in Table 4.4. A 15-pin connector located at the rear of the unit is utilized for this interface.

4.4.1 Interface Output Drivers

Levels - Zero to 3 volts

Binary one - 4V ±1 volt

Binary zero - 0V ±0.4 volts

Impedance - 100Ω ±5%

Protection - Outputs protected against short circuits to ground

4.4.2 Interface Input Receivers

Binary one - 4V ±1 volt

Binary zero - 0V ±0.4 volts

Impedance - 1000Ω ±5%

Protection - -1.5V to +7V without damage to receiver circuits.

The input/output signal pin assignments are listed in Table 4.4.

TABLE 4.4

DTL/TTL CONNECTOR PIN ASSIGNMENTS

PIN	CODE	NAME	DESCRIPTION
1	ORN	Frame Ground	Frame Ground
2	BLU	Transmit Data	An Output
3	YEL	Receive Data	An Input
4	RED	Request to Send	An Output
5	BLK	Receive Clock	An Input
6	BRN	Transmit Clock	An Input
7	GRN	Signal Return	0 volts reference.
8	WHT	Data Terminal Ready	An Output
9-15	---	(Not Used)	---

5.0 OPTIONS

5.1 Carrying Cases

Two types of carrying cases are available for the Models 1300/1310. Both are shown in Figure 5.1.

An aluminum case is designed for heavy duty handling. This unit is constructed of aluminum and is lined internally with a foam insert exactly fitted to the Models 1300/1310. A compartment for cords and miscellaneous accessories is provided. This unit may be shipped with complete safety as airline luggage. This carrying case also has a lock.

An attache type carrying case of heavy duty molded plastic is also available. This case is fitted with foam padding contoured to the Models 1300/1310. A compartment for cords is provided and the case can be locked.

5.2 Rack Mount

A rack mount adapter is available for mounting the Models 1300/1310 in a 19" wide rack. A Model 1310 is shown mounted in such an adapter in Figure 5.2. The rack mount adapter consists of a 5¼" (13.34 cm) high x 19" (48.26 cm) wide plate with a window cut out. The test set is installed in this rack mount adapter plate by removing the handle and simply slipping the test set through the window. Two connectors are mounted on the front panel of the rack mount adapter and labeled To DTE and To DCE, respectively. These connectors are plugged into the associated connectors located on the rear panel of the test set, thus enabling the operator to plug the test set into a modem (DCE) or TDM port (DTE or DCE) from the front panel. This is useful when incorporating the test set in a tech control center where all EIA interfaces are brought out to the front panel.

5.3 Divide Data Rate by 3

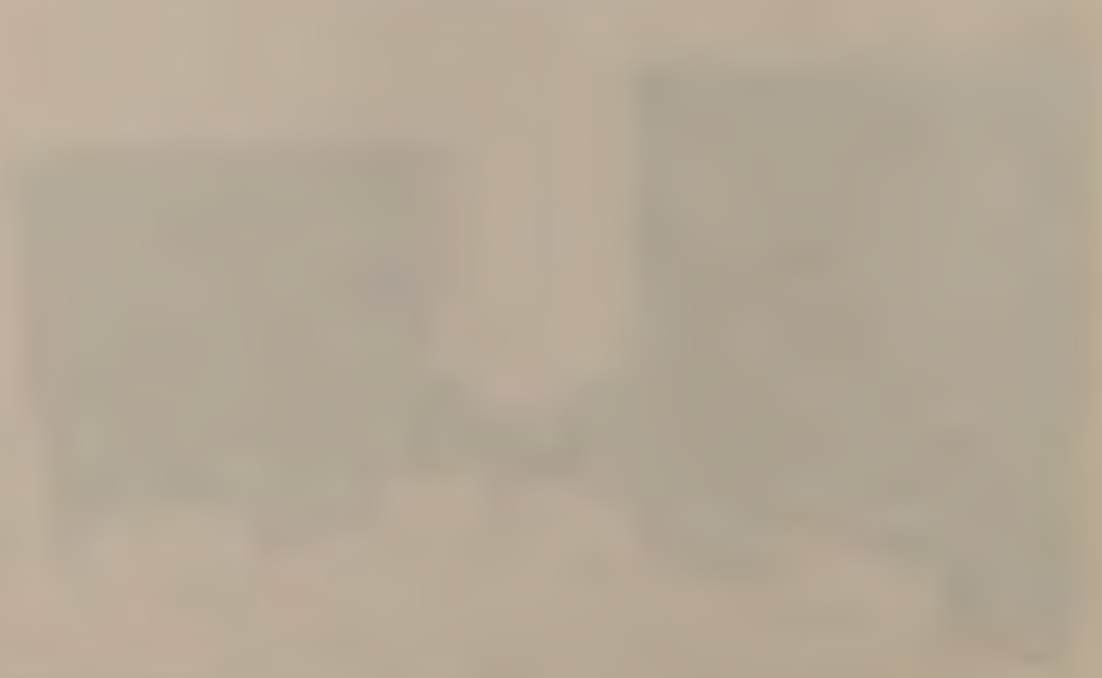
This switch allows the operator to divide all the selected Data Rates by 3, except the EXT data rate.

5.4 TTY Interfaces: 2 ma, 20 ma, or 60 ma (Neutral)

The TTY interface options allow the test set to operate with 2, 20, or 60 milliamp interfaces.

The test set can also operate with the standard EIA interfaces and a switch labeled TTY/OFF allows the operator to select between the two. The TTY input and output circuits are energized only when this switch is in the position labeled TTY.

FIGURE 5.1 ATTACHE (TOP) AND ALUMINUM (BOTTOM) CARRYING CASES FOR THE MODELS 1300 AND 1310 TEST SETS.



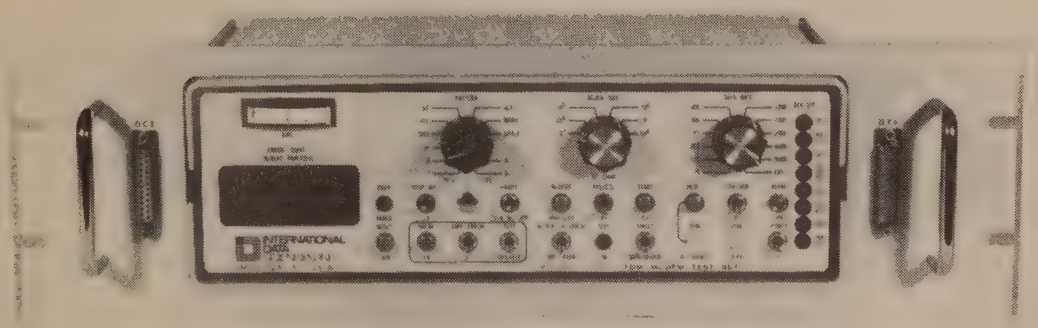


FIGURE 5.2 TEST SET MOUNTED IN A RACK-MOUNT ADAPTER.

5.4 TTY Interfaces: 2 ma, 20 ma, or 60 ma (Neutral) (continued)

Send Data and Receive Data lines are connected to the test set by means of a terminal block mounted on the rear of the test set. The terminal block has two screws to connect the Receive Data (labeled RD) Tip and Ring (labeled T and R) leads. A second pair of screws in this terminal block are used to connect the Send Data (labeled TD) Tip and Ring (labeled T and R) leads.

SPECIFICATIONS

Receive Data....Mark: Must supply 20 milliamps (in the 20 ma or 20 ma option) or 60 milliamps (in the 60 ma option) into a 100 ohm load.

Space: Open Circuit

Send Data.....Mark: Switch closure capable of looping 20 milliamps (in the 2 ma or 20 ma option) or 60 milliamps (in the 60 ma option).

Space: Capable of withstanding up to 60 volts across the Tip and Ring Terminals in the space condition.

Isolation.....All input and output leads have a 1 megohm or greater isolation to ground. All input and output circuits are optically isolated.

5.5 External Timing for Current or V.35 Interfaces

This option applies only if the unit is equipped with the Current Interface option (described in Section 4.1) or the V.35 Interface option (described in Section 4.3) or both. If both options are included, only one frequency 50 Kbps or 56 Kbps can be selected.

5.5.1 Operation with Current Interface

This option supplies a transmit clock on Pin H of the Burndy connector (see Table 4.1) to the modem at 50 Kbps or 56 Kbps as specified at time of purchase.

5.5.2 Operation with V.35 Interface

This option supplies a balanced Transmit Clock on Pins U and W of the modem connector (see Table 4.3) at 50 Kbps or 56 Kbps as specified at time of purchase.

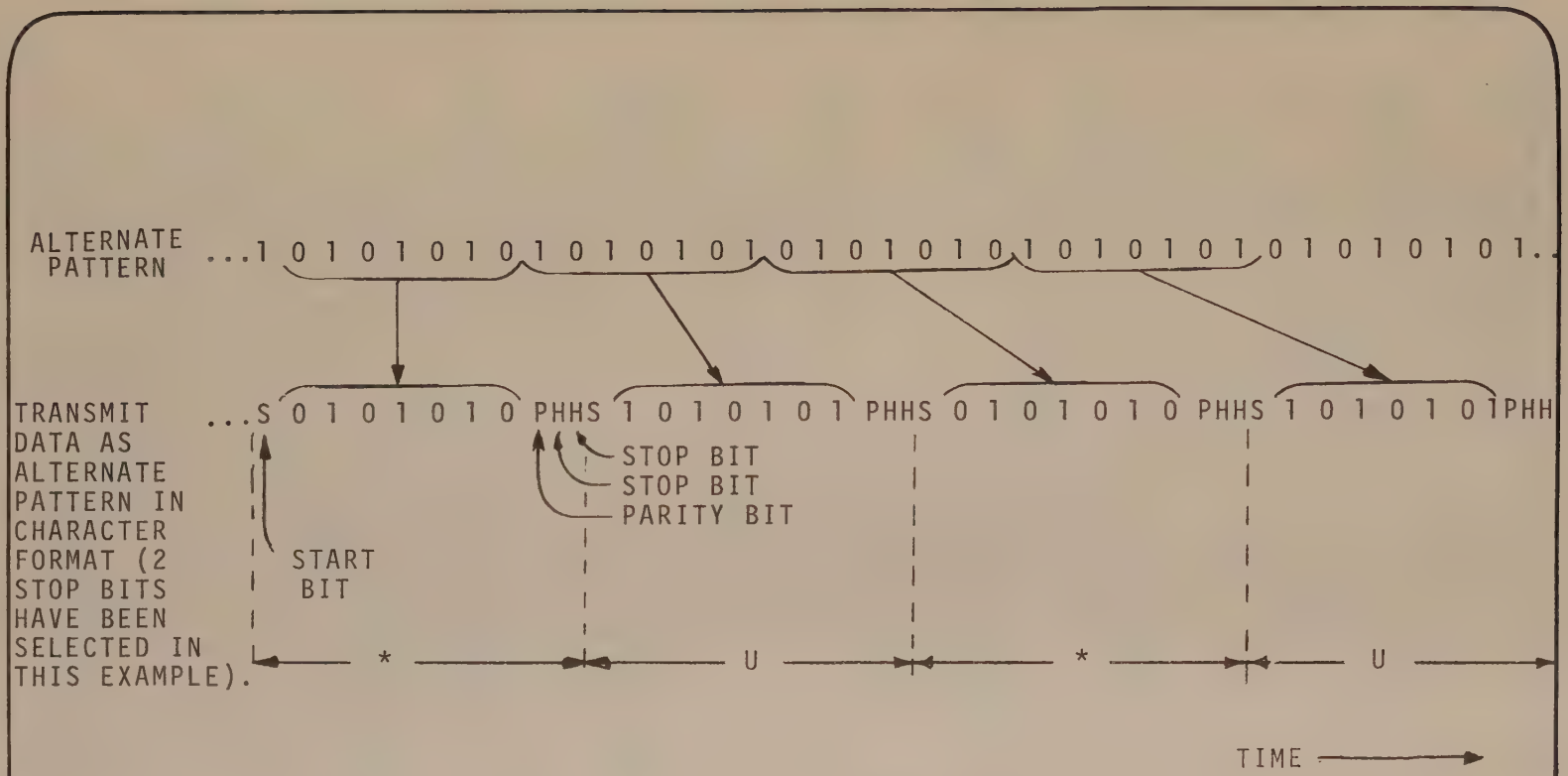
6.0 APPLICATIONS

6.1 U, * Repeating Pattern

It is possible to generate a character pattern consisting of repeating U, *, characters in the ASCII code. This is accomplished by setting the following switches on the front panel of the Model 1300 or 1310.

1. Data Rate switch to desired rate.
2. Sync/Async switch (Model 1310 only) to Async.
3. Pattern switch to ALT.
4. Character Code Level switch to 7.
5. Stop Bits switch to 1, 1.4, or 2.
6. Parity switch to Even, No, or Odd.
7. Test-Operate switch to Operate.
8. DTR/DSR Off to DTR/DSR.
9. RTS/CTS-Off to RTS/CTS

Figure 6.1 illustrates how the alternate mark-space pattern is transformed by the test set into a U, * repeating pattern in ASCII code.


ALTERNATE PATTERN
...1 0 1 0 1 0

7.0 TEST PROCEDURE

Before turning M1310 on, set switches to the following positions:

```
     Single/Continuous  -  Continuous
            Sync/Async  -  Async
             Data Rate  -  9600
          Test/Operate  -  Test
            Code Level  -  8
               Pattern  -  63
        Bit/Block Error  -  Bit
               RTS/CTS  -  ON
```

All other switches off or inactive.

1) Power on reset test in character mode.
   Turn power on.

```
        NOTE:  Sync Recovered lamp  -  OFF
                  Sync Locked lamp  -  ON
                       Error Count  -  000
                    Over Range lamp  -  OFF
                TC, RD, RC, TD LEDs  -  ON
                     All other LEDs  -  OFF
```

2) Check power supply voltages

```
  +5 VDC = 4.75 - 5.25
 +12 VDC = 11.4 - 12.6
 -12 VDC = -12.6 - -11.4
```

3) Power on reset test in infinity mode.

```
       Power  -  OFF
  Code Level  -  ∞
      Repeat Step 1
```

4) Bias Meter adjustment and check.
   Pattern switch - ALT
   NOTE: Sync Locked lamp On
   Adjust R7 on A1 board for a zero meter reading.

5) Pattern switch - Space
   NOTE: Meter reads - S
   Sync Locked lamp - OFF

6) Pattern switch - Mark
   NOTE: Meter reads - M
   Sync Locked lamp - ON
   Sync Recovered lamp - ON
   Reset Sync - depress and release
   Observe: Sync Recovered lamp - OFF

7) Bit/Block Error selection test.
Pattern - 63
Break Sync - Depress and Release
NOTE: Error Counter advances rapidly; then resets to 000.
Sync Locked lamp - ON
Sync Recovered lamp - ON

8) Repeat Step 7 for Patterns 511 and 2047.

9) Block Size - 10^3
Bit/Block Error - Block
Break Sync - Depress and Release
NOTE: Error Counter advances noticeably slower.
Sync Locked lamp - ON
Sync Recovered lamp - ON

10) Repeat Step 9 for Patterns 511 and 63.

11) Check Start/Stop Patterns.
Bit/Block Error - Bit
Code Level - 8
Break Sync - Depress and Release
NOTE: Sync Locked lamp - ON
Sync Recovered lamp - ON
Error Count - 000

12) Repeat Step 11 for Code Levels 7, 6, and 5.

13) Check for Error Count in Start/Stop mode.
Xmit Errors - ON
Single/Continuous - Single
Reset Count - depress and release
Start Test - depress and release
Observe: 1) Test End lamp is off while test is running and lights when test is through.
2) Error Count = 16 ±1
Blocks Analyzed - depress
Observe: Blocks Analyzed = 1
Blocks Analyzed - release

14) Bit/Block - Block
Reset Count - Depress and Release
Start Test - Depress and Release
Observe: Test End lamp - goes off then comes on again.
Error Count = 79 ±1

Blocks Analyzed - depress
Observe: Blocks Analyzed = 1
Blocks Analyzed - release

15) Code Level - 6
Repeat #14
Observe: Error Count = 95 ±1
Blocks Analyzed = 1

16) Code Level - 7
Repeat #14
Observe: Error Count = 111 ±1
Blocks Analyzed = 1

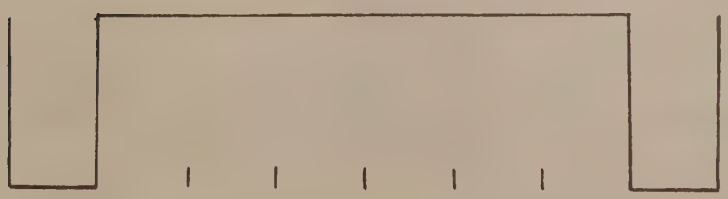
17) Code Level - 8
Repeat #14
Observe: Error Count = 127 ±1
Blocks Analyzed = 1

18) Code Level - ∞
Repeat #14
Observe: Error Count = 1
Blocks Analyzed = 1

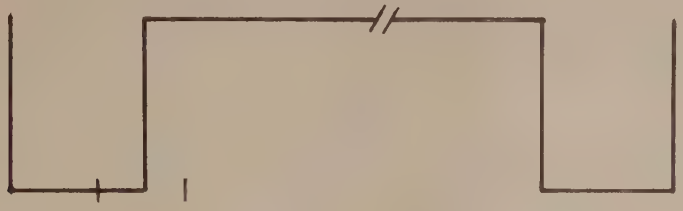
19) Check Stop Bits and Parity.

Xmit Errors - OFF
Test/Operate - Operate
Pattern - Space
Code Level - 5
Bit/Block Error - Bit
Stop Bits - 1
Parity - No
Single/Continuous - Continuous

Connect scope to DCE connector Pin 2 (TD).
NOTE: Scope @ .1ms/cm. Adjust variable so that each gradual is one bit wide.



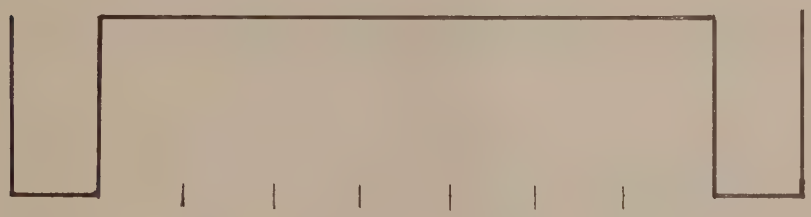
Stop Bits - 1.4



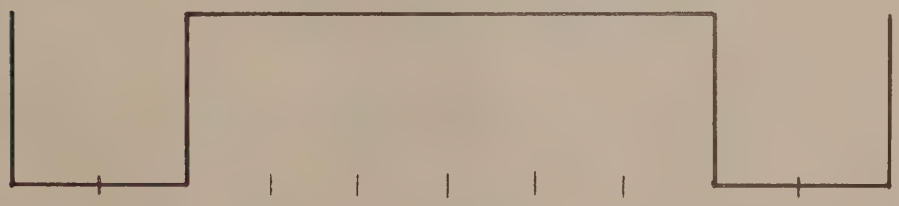
Stop Bits - 2

Stop Bits - 1

Parity - Even



Parity - Odd



20) Repeat Step 19 for code levels 6, 7, and 8. Add one Bit of data for each successive stop.
NOTE: Observe length of character increasing by one bit for each test.

21) Code Level -
Data Rate - EXT
NOTE: All LEDs - OFF

22) Reset Count switch - Depress
NOTE: All LEDs - ON
Reset Count switch - Release

23) Pattern Switch - 63
Check Error Count and Blocks Analyzed circuits.
Loop Transmit Data (DCE Pin 2) to Receive Data.
Connect a square wave generator to DCE Pins 15 and 17.
NOTE: Generator output is a 1 KHz signal at ±6V.
Bit/Block Error - Block
Xmit Error - ON
NOTE: First reset Error Count, then each time the units column advances, depress the Blocks Analyzed push-button switch and insure that the Error Count numbers and the Block Analyzed numbers are the same.

24) Generator - 10KHz
Repeat Step 23 for the tens column.

25) Generator - 100KHz
Repeat Step 23 for the hundreds column.
NOTE: Insure that the Over Range lamp for both counters lights at the appropriate time, and then reset the error count and insure that the lamp goes off for both counters.

26) Check Block Size
NOTE: Increase external generator to maximum frequency which the unit stays in sync.

Bit/Block - Bit
Single/Continuous - Single
Reset Count - Depress and release
Start Test - depress and releast

Observe: 1) Test End lamp will be off while test is running, and will come on when test is finished.
2) Error Count = 16 ±1

Blocks Analyzed - depress
Observe: Blocks Analyzed = 1
Blocks Analyzed - release

27) Block Size - 10^4
Reset Count - depress and release
Repeat #26
Observe: Error Count = 159 ±1
Over Range lamp - Off
Blocks Analyzed = 1

28) Block Size - 10^5
Reset Count - depress and release
Repeat #26
Observe: Error Count = 587 ±1
Over Range lamp - ON
Blocks Analyzed = 1

29) Block Size - 10^6
Reset Count - depress and release
Repeat #26
Observe: Error Count - 873 ±1
Over Range lamp - On
Blocks Analyzed = 1

30) Block Size - 10^7
Reset Count - depress and release
Repeat #26
Observe: Error Count = 730 ±1
Over Range lamp - On
Blocks Analyzed = 1

31) Block Size - 10^8
Reset Count - depress and release
Repeat #26
Observe: Error Count = 301 ±1
Over Range lamp - On
Blocks Analyzed = 1

32) Block Size - 10^3
Single/Continuous - Continuous
Xmit Errors - Off

33) EIA Receiver Thresholds Test

Generator - 10KHz
Connect Generator - to DCE Pin 3 (Disconnect from Pin 2)
NOTE: Generator set at 10KHz

NOTE: By varying the Generator DC offset and monitoring the front panel LED (RD) insure that the threshold is _ 1.5V.

34) Connect Generator output to DCE Pin 15 (TC, TD) and repeat Step 33.

35) Connect Generator output to DCE Pin 17 (RC) and repeat Step 33.

36) LED Check
Pattern - Space
Connect Generator to:

DCE Pin	15	and only the	TC LED will light
"	17	"	RC "
"	3	"	RD "
"	5	"	CTS "
"	6	"	DSR "
"	8	"	DCD "
"	21	"	SQ "

37) Check for ground at DCE Pins 1 and 7.

38) Check Data Output.
Pattern - 63
Data Rate - 9600
Scope - DCE Pin 2
NOTE: Observe data at ±6V ±.5V.

39) RTS/CTS - Off
Scope - DCE Pin 2
Observe - 6V ±.5V

40) Check RTS Output
RTS - On, DCE Pin 4 at +11V ±1V
RTS - Off, DCE Pin 4 at -11V ±1V

41) Check DTR Output
DTR - ON, DCE Pin 20 at +11V ±1V
DTR - OFF, DCE Pin 20 at -11V ±1V

42) Check SCTE (DCE Pin 24)
NOTE: Output Level +6V ±1V
RC LED - ON

43) Sync/Async - Sync
NOTE: 1) DCE Pin 24 output is a square wave at 9600 Hz at ±6V ±.5V.
2) RC LED Off

44) Check DTE connector Pins 1 and 7 for ground.
Sync/Async - Async

45) With Scope on DTE Pin 2, gen. into DCE Pin 3, observe gen. output
" 4 " 5 "
" 20 " 6 "

46) With Scope on DTE Pin 5 and RTS switch on observe +11V ±1V.
With Scope on DTE Pin 5 and RTS switch off observe -11V ±1V.
RTS Switch - ON

47) With Scope on DTE Pin 6 and DTR switch on observe +11V ±1V.
With Scope on DTE Pin 6 and DTR switch off observe -11V ±1V.

48) With Scope on DTE Pin 3 observe data (±6V ±1V).

49) Pattern Mark
Connect DCE Pin 3 to DCE Pin 20.
NOTE: Observe that when DTR switch is turned on, the Error Count advances one number and when DTR switch is turned off, the Error Count does not change.

50) Check Option Connector

Pin 24 - Pattern switch - 63
Test/Operate - Test
Xmit Errors - ON
Break Sync - Depress and Release

NOTE: Positive pulse 2 to 8 ms long during loss-of-sync. (Sync Locked Lamp Off)

Pin 23 - Observe on scope positive pulses with 6.5ms between them.

Pattern switch - 511
Observe positive pulses with 54 ms between them.
Pattern switch - 2047
Observe positive pulses with 220ms between them

Pin 22 - Square wave at TTL level.

Pin 21 & 25 - Check for ground.

Pin 20 - Check for data at ±6V ±1V.

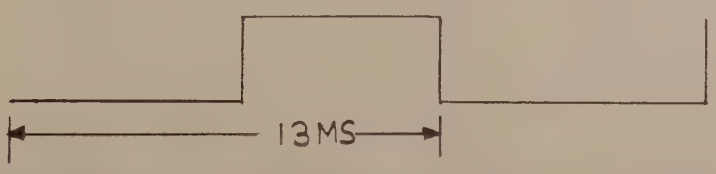
Pin 19 - When the Sync Recovered lamp is on this will be Ov. When Sync Recovered lamp is off the level will be 4V ±.5V.

Pin 18 - Pattern switch - 63
Note: Data at ±6V ±1V.
Pattern switch - ALT
Note: Square Wave at ±6V ±1V.
Pattern switch - Mark
Note: Signal at -6VDC ±1V.
Pattern switch - Space
Note: Signal at +6VDC ±1V.

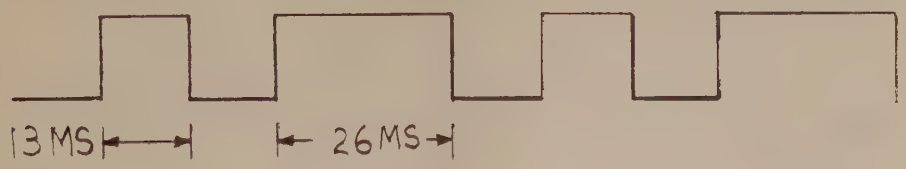
Pin 17 - Pattern switch - 63
Reset Count switch - Depress
NOTE: Signal at OV.
Reset Count switch - Release
NOTE: Signal at +5V ±1V.

Pin 16 - Square Wave at TTL level.

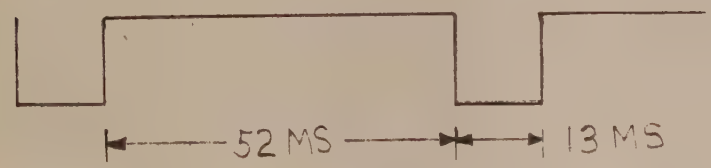
Pin 15 - Pattern switch - 63



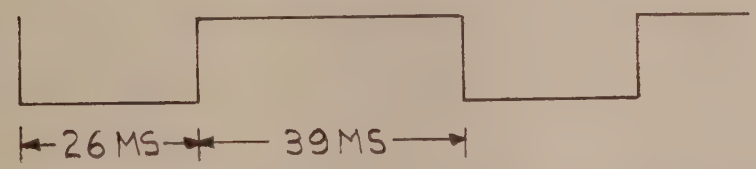
Pin 14 -



Pin 13 -

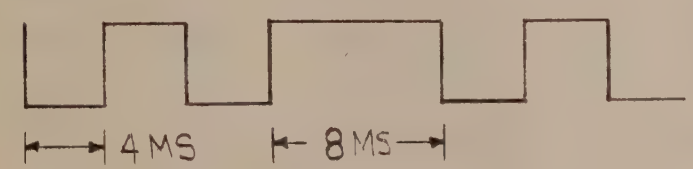


Pin 12 -

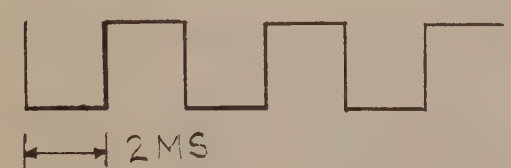


On the following pins (11-4) to observe the waveforms, the Break Sync switch will have to be depressed and released each time.

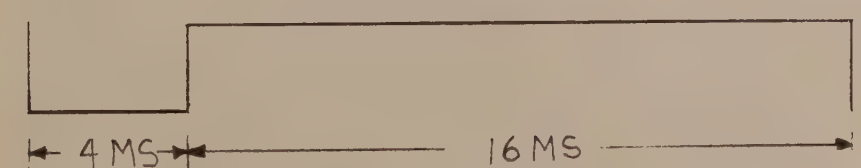
Pin 11 -



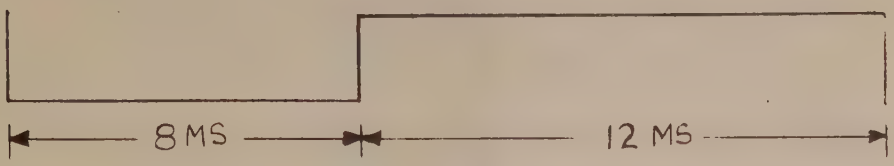
Pin 10 -



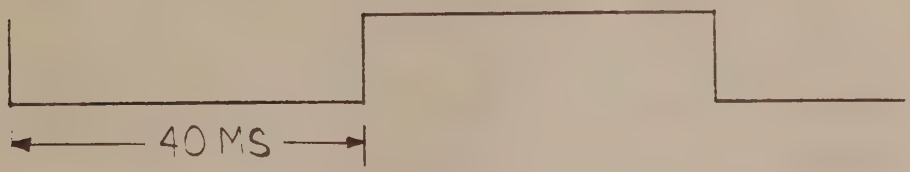
Pin 9 -



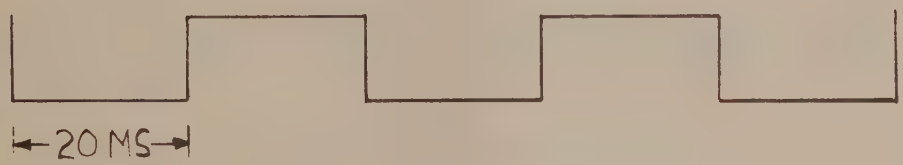
Pin 8 -



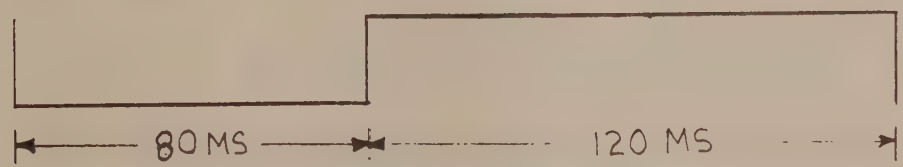
Pin 7 -



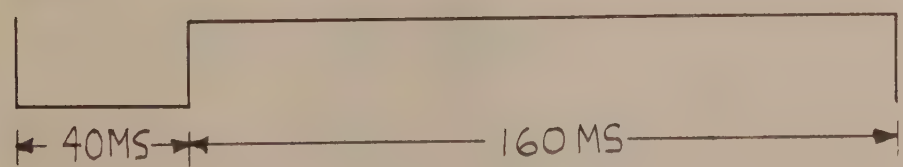
Pin 6 -



Pin 5 -



Pin 4 -



Pin 3 - Break Sync switch - Depress
NOTE: Signal at 0V.
Break Sync switch - Release
NOTE: Signal at 4V ±.5V.

Pin 2 - Observe negative pulses with 6.5ms between them.
Pattern switch - 511
Observe pulses with 54ms between them.
Pattern switch - 2047
Observe pulses with 220ms between them.

Pin 1 - Observe positive pulses with 220ms between them.
Pattern switch - 511
Observe pulses with 54ms between them.
Pattern switch - 63
Observe pulses with 6.5ms between them.

51) Connect frequency counter to Pin 16 of option connector. Rotate Data Rate switch counter clockwise from positions 9600 through 600.
NOTE: At each data rate, counter will agree with front panel knob location ±.1%.

From Data Rate 300 to 75 continue same process but also depress and release Break Sync switch and observe that Error Counter never advances beyond 700 in each rate before it gets back into sync.

52) Plug M1310 into Variable Transformer and vary A.C. input from 100 VAC to 130 VAC and observe that the unit never loses sync.

NOTE: The following tests incorporate a special test set up using a modified IDS M1200 and a modified IDS M9150.

53) Clock Recovery
With modified IDS M1200 in the HI position and Data Rate 9600 connect to M1310 DCE connector.
On M1310
Data Rate switch - 9600
Test/Operate switch - Operate
Pattern switch - 2047

NOTE: Test is passed if after one minute the M1310 has not lost sync or counted errors.

Modified M1200 to LO position.
Reset Sync Recovered switch - Depress and Release
NOTE: Test is passed if after one minute the M1310 has not lost sync or counted errors.

54) Full Duplex test
Modified M1200 Data Rate switch - EXT
M1310 Data Rate switch - EXT
Depress and release Reset Sync Recovered switch.
NOTE: Test is passed if after five minutes the M1200 and M1310 have not lost sync or counted errors.

APPENDIX

The Appendix includes the following schematics:

Model 1310 Schematic A1 Board & Parts List

Model 1310 Schematic A2 Board & Parts List

Model 1310 Schematic Start/Stop A3 Board & Parts List

Model 1310 Interconnection Diagram & Parts List

PL: E-250167

1200/1300 SERIES 1310	
MODEL NO.	NEXT ASSEMBLY

	NAME:	DATE:
COMPILED	T. Grant	10/24/72
CHECKED	D. Courtois	11/13/72
APPROVED	R. J. Stout	11/13/72

INTERNATIONAL DATA SCIENCES, INC.
PROVIDENCE, R.I., U.S.A.

IDENTIFICATION CODE: 50572

PL E-250167

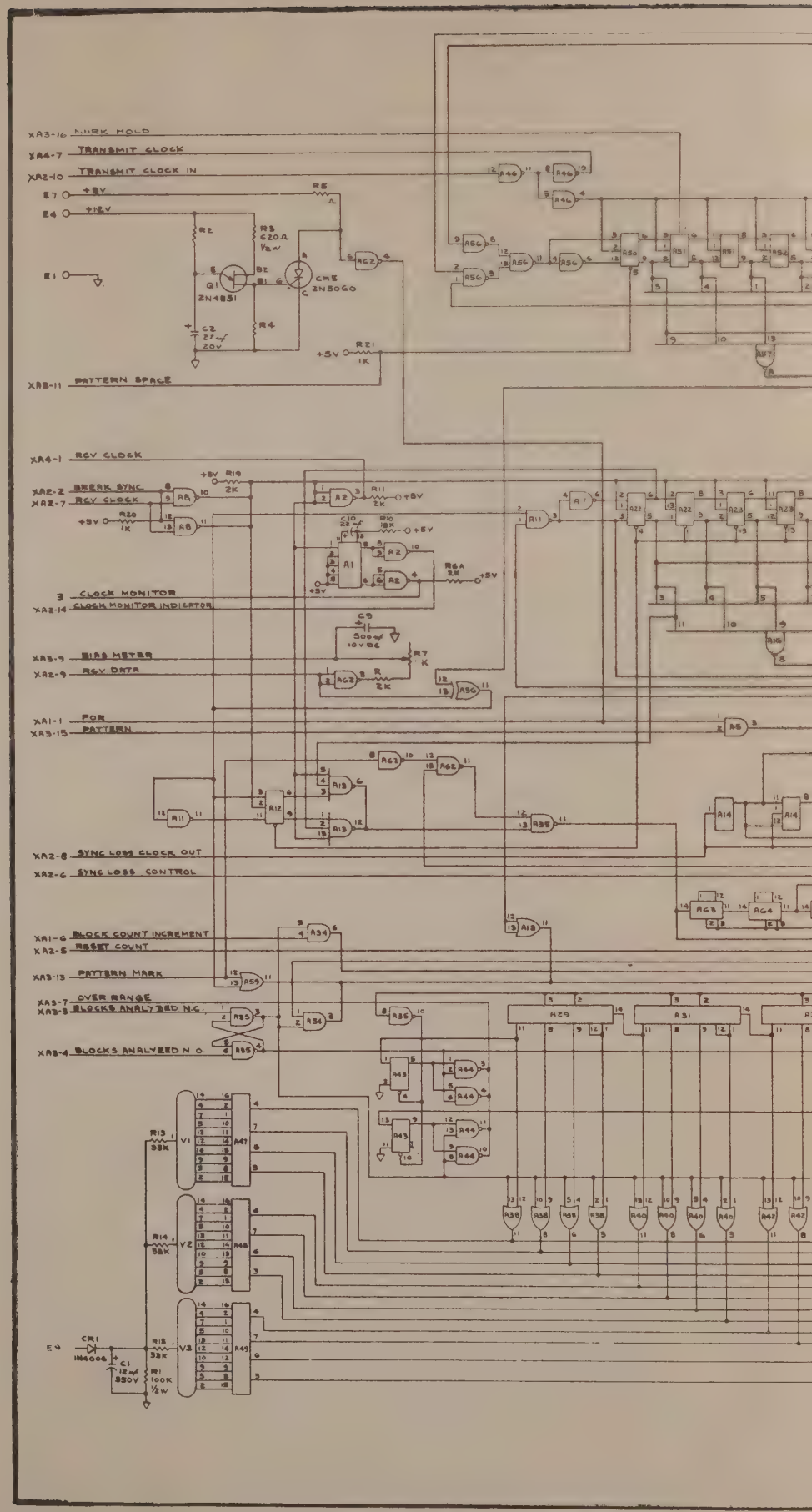
SHEET 1 OF 4 REV.

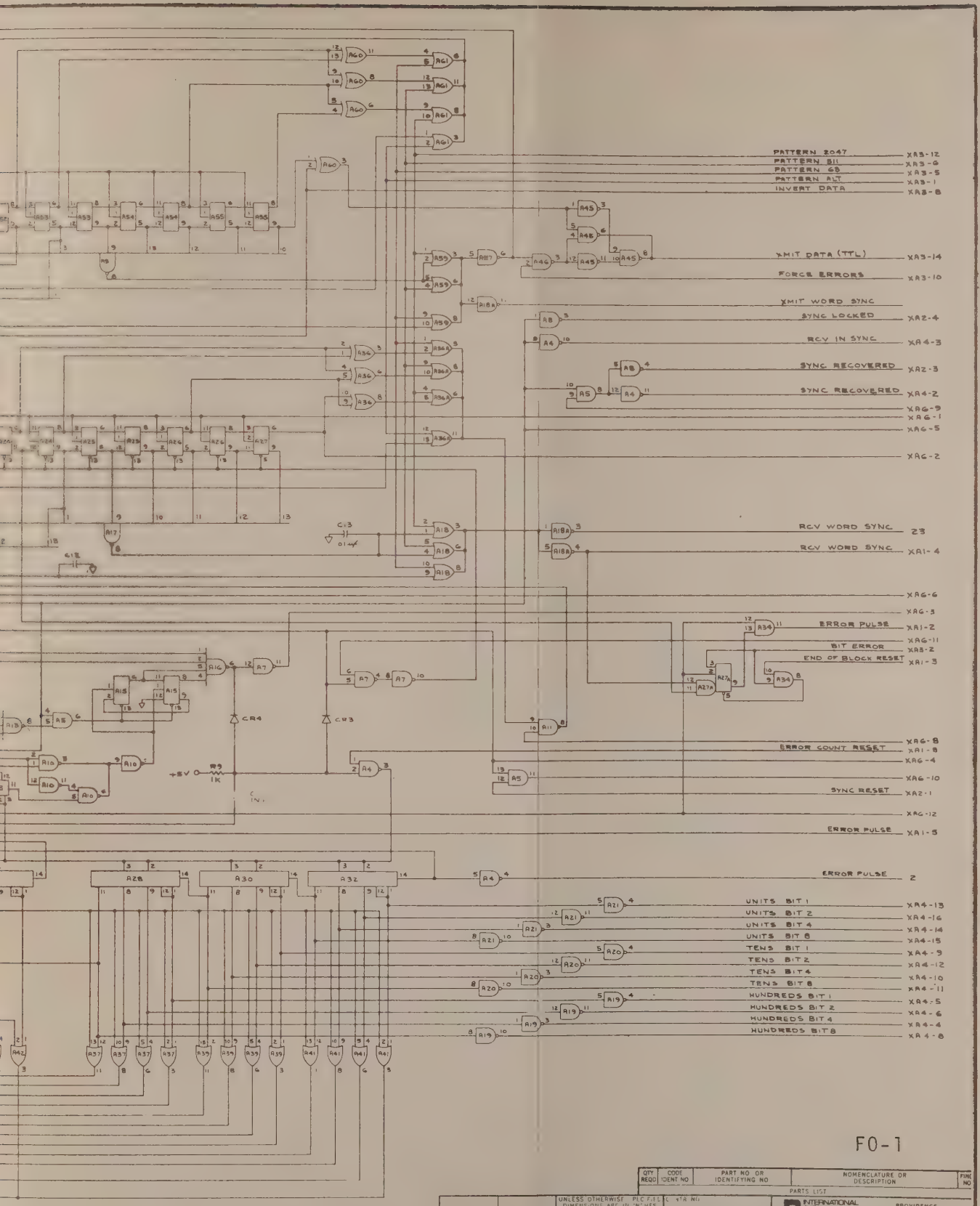
TITLE:
A1 BOARD ASSEMBLY
MODEL 1200/1300 SERIES

LTR	REVISION DESCRIPTION	DATE	APPD
Q	Retyped without Change	4/18/75	N.P.
R	REVISED VALUE OF C12 PER ECO 57-75	4/28/75	N.P.
S	REVISED ITEMS C11, C12 & C13 PER ECO 114-75	9-26-75	
T	CHAN REF NO. ADDED 1310 TO SERIES NO FOR SCHEMATIC ECO-19-76	3-3-76	
U	REV R9 PART NO. ECO 102-76	8-6-76	N.P.
V	R2 WAS 8.2K ½W, R4 WAS 10Ω ½W REVISED PER ECO 25-77	4-14-77	
W	REVISED R5 ECO 27-77	4-22-77	N.P.

LTR	REVISION DESCRIPTION	DATE	APPD

UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 WATT COMPOSITION, STYLE RC07
ALL CAPACITORS ARE CERAMIC, STYLE CK05


XA3-16 MARK HOLD
XA4-7 TRANSMIT CLOCK
XA2-10 TRANSMIT CLOCK IN
E7 +8V
E4 +15V
E1
R5 4.7Ω
R2
R3 620Ω ½W
Q1 2N4851
CR5 2N5060
C2 22µF 20V
R4
+5V R21 1K
XA3-11 PATTERN SPACE
XA4-1 RCV CLOCK
XA2-2 BREAK SYNC
XA2-7 RCV CLOCK
+8V R19 2K
R20 1K
R11 2K
C10 22pF
R10 18K
R6A 2K
3 CLOCK MONITOR
XA2-14 CLOCK MONITOR INDICATOR
C9 500µF 10V DC
XA3-9 BIAS METER
XA2-9 RCV DATA
R7 K
R 2K
XA1-1 POR
XA3-15 PATTERN
XA2-8 SYNC LOSS CLOCK OUT
XA2-6 SYNC LOSS CONTROL
XA1-6 BLOCK COUNT INCREMENT
XA2-5 RESET COUNT
XA3-13 PATTERN MARK
XA3-7 OVER RANGE
XA3-5 BLOCKS ANALYZED N.C.
XA3-4 BLOCKS ANALYZED N.O.
R13 33K
R14 33K
R15 33K
V1
V2
V3
E9
CR1 IN4004
C1 12µF 350V
R1 100K ½W



FO-1

QTY REQD	CODE IDENT NO	PART NO OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	FIND NO
PARTS LIST				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

DR T. GRANT 10-13-74
CHK
APD

APPROVED
BY DIRECTION OF

NEXT ASSY | USED ON
APPLICATION

INTERNATIONAL DATA SCIENCES, INC
PROVIDENCE RHODE ISLAND

DRAWING TITLE MODEL 1310 SCHEMATIC A1 BOARD

SIZE	CODE IDENT NO	DRAW NO NO	REV
E	50572	250269	G

SCALE
SHEET 1 OF 1

PL E-250167 1310/1200/1300 SERIES SH 2

REF. DES/ ITEM NO.	QTY	PART NO.	VALUE	DESCRIPTION	VENDOR	REMARKS	CODE
		E-250167		Assembly		Printing W.Board	
1	1	E-250168		Detail		" " "	
A1	1	SN9601N		Integrated Circ.	Stuart Warner		
A2, A8, A44	3	MC858P		" "	Motorola		
A4, A7, A18A A19,	9	MC857P		" "	"		
A20, A21, A35 A46, A62							
A5, A9, A34	3	MC1807P		" "	"		
A10, A11, A45	4	MC849P		" "	"		
A56							
A12, A27A, A27, A50	4	MC845P		" "	"		
A13	1	MC863P		" "	"		
A14, A15, A23 A24, A25, A26							
A54, A55 A51, A52, A53	11	MC855P		" "	"		
A16, A57	2	MC1801P		" "	"		
A17, A58	2	MC1805P		" "	"		
A18, 36A, A37, A38,							
A39, A40, A41, 42, 59, 61	10	MC1809P		" "	"		
A6, A43	2	MC856P		" "	"	USE A6 WITH XA6	

PL E-250167 MODEL 1200/1300/1310 SH 3

REF. DES/ ITEM NO.	QTY	PART NO.	VALUE	DESCRIPTION	VENDOR	REMARKS	CODE
A28,A29,A30, A31,A32,A33, A63,A64,A65	9	SN7490N		Integrated Circ.	Texas Instru.		
A36, A60	2	SN7486P		" "	Texas Instru./ National		
A47, A48, A49	3	SN74141N		" "			
A22	1	MC3062P		" "	Motorola		
C1	1	TVA1605	12uf350V	CAP, Electrolytic	Sprague	or Cornell Dub. WBR 12-350	
C2, C10	2	CS13BD226K	22uf 20V	CAP, Tant.	"		
C9	1	WBR-500-16	500uf16V	CAP, Electrolytic	Cornell Dubilier		
C11, C13,	2	UK25-103	.01uf	Capacitor	Kemit		
C12	1	DD391	390 pf	"			
CR1	1	1N4006		Diode	Motorola		
CR5	1	2N5060		SCR	"		
Q1	1	2N4851		Transistor	"		

PL E-250167 MODEL 1200/1300/1310 SH 4

REF. DES/ ITEM NO.	QTY	PART NO.	VALUE	DESCRIPTION	VENDOR	REMARKS	CODE
R1	1	RC20GF104J	100K ½w	Res.			
R2	1		20K ½W 5%	"			
R3	1	RC20GF621J	620Ω ½w	"			
R4	1		27Ω ½W 5%	"			
R5	1	RCR32G510J	51Ω 1W 5%	"	ALLEN BRADLY		
R7	1	3339H-1-502	5K ½w	Trimpot	Bourns		
R8, R11, R16A	4	RC20GF202J	2K ½w	Res.			
R10	1	RC20GF183J	18K ½w	"			
R13, R14 R15	3	RC20GF333J	33K ½w	"			
R16, R20 R21,	3	RC20GF102J	1K ½w	"			
R9	1	RC07GF102J	1K 1/4w	"			
V1, V2, V3	3		B5440	Nixie Tubes	Burrough		
XA2, XA3, XA4	3	931600R716-2		16 Pin Socket	T.I. Vector		
XV1, XV2, XV3	3	SK196		Nixie Sockets	Burrough		
XA1, XA6	2	931400R714-2		14 Pin Socket	T.I. Vector		
REF		E-250269		Schematic			
REF		A250167		Visual Aid			
REF		C-250109		Final Assembly Drawing		A1 Board	
REF		E-250169			Artwork		

PL: E-250160

1300/1310	
MODEL NO.	NEXT ASSEMBLY

	NAME:	DATE:
COMPILED	M. Suibielski	10-12-72
CHECKED	R.J. Stout	11-09-72
APPROVED	A. Lucci	11-09-72

INTERNATIONAL DATA SCIENCES, INC.
PROVIDENCE, R.I., U.S.A.

IDENTIFICATION CODE: 50572

PL E-250160 | Y

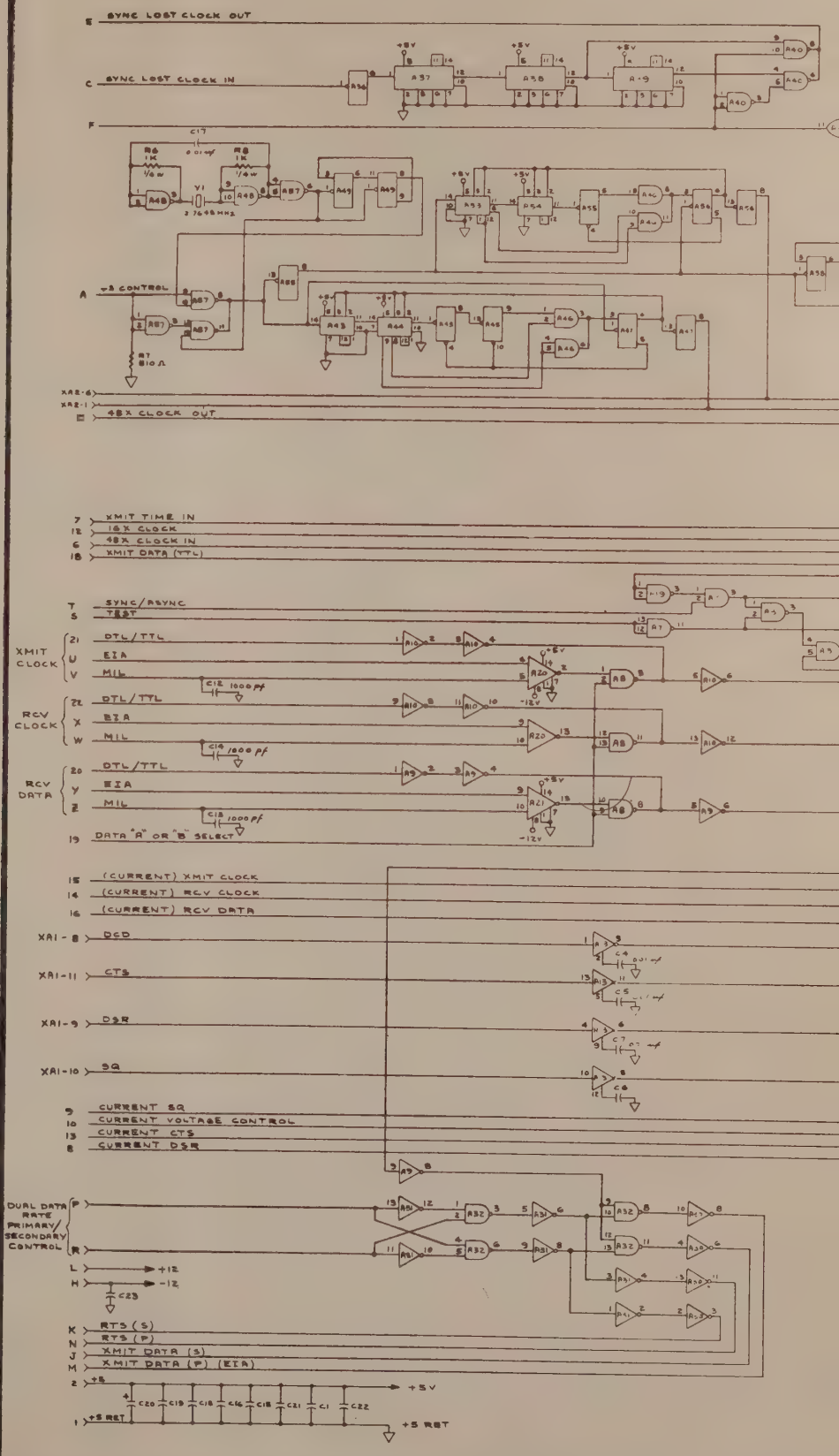
SHEET 1 OF 3 | REV.

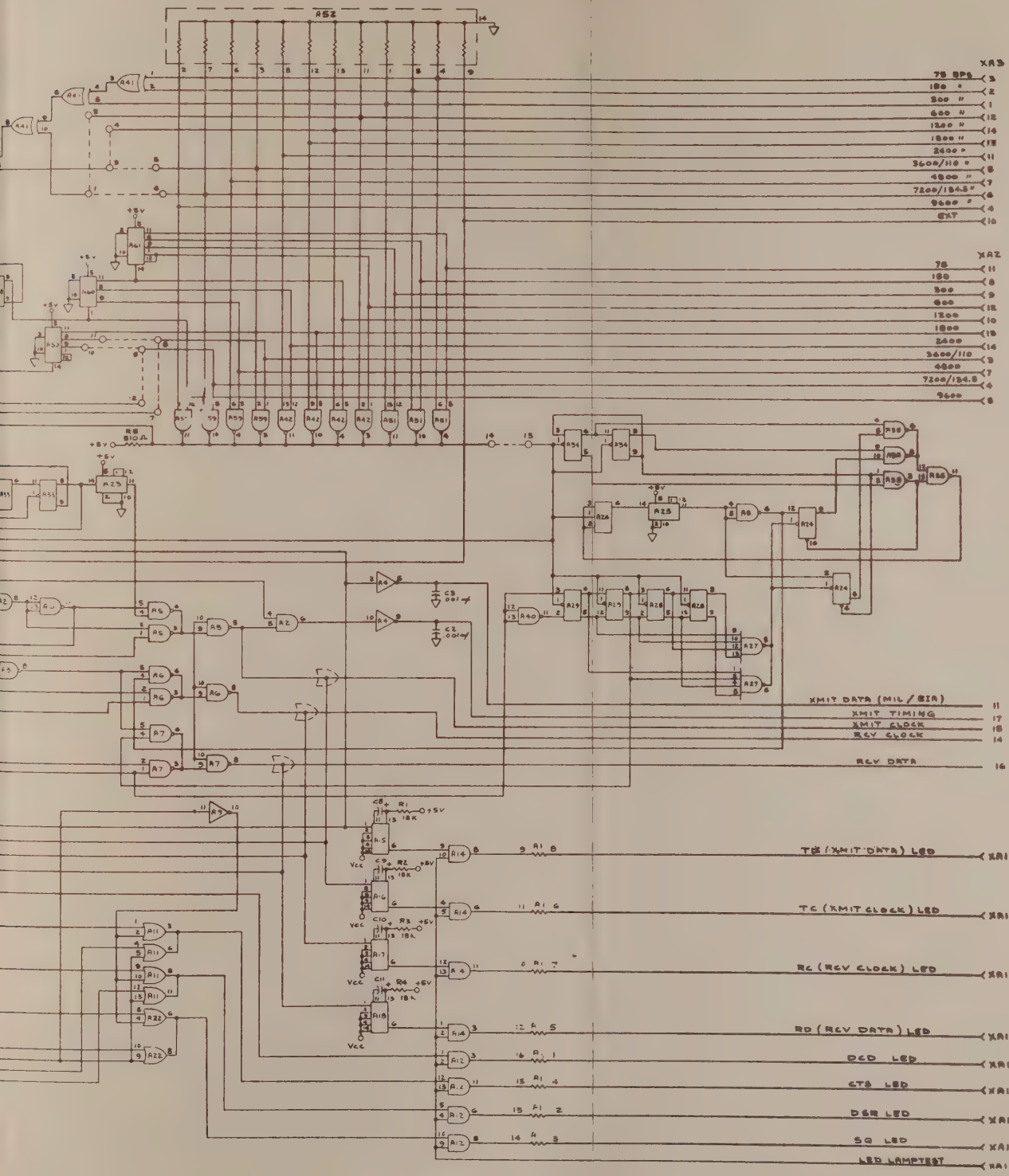
TITLE: A2 BOARD

LTR	REVISION DESCRIPTION	DATE	APPD
W	Retyped Without Change	4/21/75	
X	REVISED ITEM C1, C5-C9, C21 & C2-C7 C12-C14, R2, ADDED XA20 & 21 PER ECO 114-75	9-26-75	
Y	MODEL 1300 TO SERIES 100, CHANGED REF NO. FOR SCHEMATIC ECO 19-76	3-3-76	

LTR	REVISION DESCRIPTION	DATE	APPD

UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 WATT COMPOSITION, STYLE RC07
ALL CAPACITORS ARE CERAMIC, STYLE CK05


E SYNC LOST CLOCK OUT
C SYNC LOST CLOCK IN
F
A -8 CONTROL
XA2-6
XA2-1
D 48X CLOCK OUT
7 XMIT TIME IN
12 16X CLOCK
6 48X CLOCK IN
18 XMIT DATA (TTL)
T SYNC/ASYNC
S TEST
XMIT CLOCK
21 DTL/TTL
U EIA
V MIL
RCV CLOCK
22 DTL/TTL
X EIA
W MIL
RCV DATA
20 DTL/TTL
Y EIA
Z MIL
19 DATA "A" OR "B" SELECT
15 (CURRENT) XMIT CLOCK
14 (CURRENT) RCV CLOCK
16 (CURRENT) RCV DATA
XA1-8 DCD
XA1-11 CTS
XA1-9 DSR
XA1-10 SQ
9 CURRENT SQ
10 CURRENT VOLTAGE CONTROL
13 CURRENT CTS
8 CURRENT DSR
DUAL DATA RATE PRIMARY/SECONDARY CONTROL
P
R
L +12
H -12
K RTS (S)
N RTS (P)
J XMIT DATA (S)
M XMIT DATA (P) (EIA)
2 +5
1 +5 RET
+5 V
+5 RET



F0-2

QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

CONTR NO
DR T. GRANT 11-6-74
CHK
APPD
APPROVED
BY DIRECTION OF

INTERNATIONAL DATA SCIENCES, INC. PROVIDENCE RHODE ISLAND

DRAWING TITLE MODEL 1310
SCHEMATIC
A2 BOARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
E	50572	250270	B

SCALE
SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	

PL E-250160 MODEL 1200 SH 2

REF. DES/ ITEM NO.	QTY	PART NO.	VALUE	DESCRIPTION	VENDOR	REMARKS	CODE
		E-250160		A2 Board Assembly			
1	1	E-250162		Printer Wiring Board		Detail	
A1	1	898-3-R220		Integrated Circ.	Beckman	Monitor Lights Option	
A2,A12,A14 A46	4	MC1807P	A2-Req'd. for Std.Bd. A2-A12, A14-A46 Req'd for Everything	Else	Motorola	A12-A14 Mon.Lt. Opt. A46-110 or 134.5	
A3,A5,A6,A7 A8,A19 [A32]					Do Not Kit		
A35,A40,A57	10	MC849P			Motorola	A32 Dual Data Rate Option	
A4	1	CM1150/N8T15A			Do Not Kit		
A9,A10 [A31]	3	MC837P			"	A31, Dual Data Rate Option	
A11,A22	2	MC1809P			"	Monitor Lights Option	
A13	1	CM1162/MC1489L			Cermetec	" "	
A15,A16,A17, A18	4	SW9601				" "	
A20, A21	2	CM1160/N8T16A		Do not Stuff before Flow Sold.	"		
A23,A25,A50, A60,A61	5	SN7493N			Texas Instru.		
A24,A28,A29, A33,A34,A49	7	MC855P			Motorola		
A58							
A26,A45,A47, A55,A56,A36	6	MC853P	A45-47,56 not Req'd for Std Bd A45,47,56 must be in for ML		"	A45,47,110 Opt. A56-134.5 Opt.	
A27	1	MC1801P			Do Not Kit		
A30	1	CM1152/MC1488L			Cermetec	Dual Data Rate Option	
A37,A38,A39 A43,A44,A53	7	SN7490N	A43,44,53,54 not req'd for Std.Bd. Must be in for M L , etc.		Texas Instru.	A43-44-110 Opt. A53,54-134.5 Opt.	
A54 A41	1	SN7486N			Motorola		
A42,A51, A59	3	MC858P		Integrated Circ.	"		

PL E-250160 MODEL 1200 SH 3

REF. DES/ ITEM NO.	QTY	PART NO.	VALUE	DESCRIPTION	VENDOR	REMARKS	CODE
A48	1	SN74L00N		Integrated Circ.	Texas Instru.		
A52	1	899-1-R330		" "	Beckman		
C1,C15,C16,C18 C19 & C21	6	UK25-103	.01uf	CAPACITOR			
C17	1	CK05BX103K	.01uf	Capacitor			
C2,3,4,5,6, 7,12,13,14	9	DD102	.001uf	"	C4,5,6,7 Mon.Lite Donot Stuff C12,13,14	C4,5,6,7 Mon.Lit. Opt.	
C8,C9,C10, C11,C20	5	CS13BD226K	22mf 15 VDC	"		Mon Lit.-Opt. C20 Always Used	
R2	1	RC07GF183J	18K	RESISTOR			
R1, R3, R4	3	RC20GF183J	18K	Resistor		Monitor Lights Option	
R5, R7	2	RC20GF511J	510 Ω	"			
R6, R8	2	RC07GF102J	1K 1/4W	"			
XA0, XA1, XA2, XA3	4	931400R714-2		14 Pin Socket	Texas Instrument Vector	XA1 MON LIT OPT ONLY	
Y1	1		2.7648 Mhz	Crystal	CTS Knight	± .005%	
C22, C23	2	CK06BX104K	.1uf	Capacitor		C23 FOR CM1160 ONLY	
REF P1	1	007-044-980-002		Connector	Elco	44 Pin	
REF1	1			Keying Pin	"		
REF		E-250161		P.C.	Artwork		
REF		E-250270			Schematic	FOR 1310	
REF		E-250159			"	FOR 1200	

PL: E-250176

1200/ 1300/1310	
MODEL NO.	NEXT ASSEMBLY

	NAME:	DATE:
COMPILED	T. Grant	1/07/73
CHECKED		
APPROVED		

INTERNATIONAL DATA SCIENCES, INC.
PROVIDENCE, R.I., U.S.A.

IDENTIFICATION CODE: 50572

PL E-250176 S

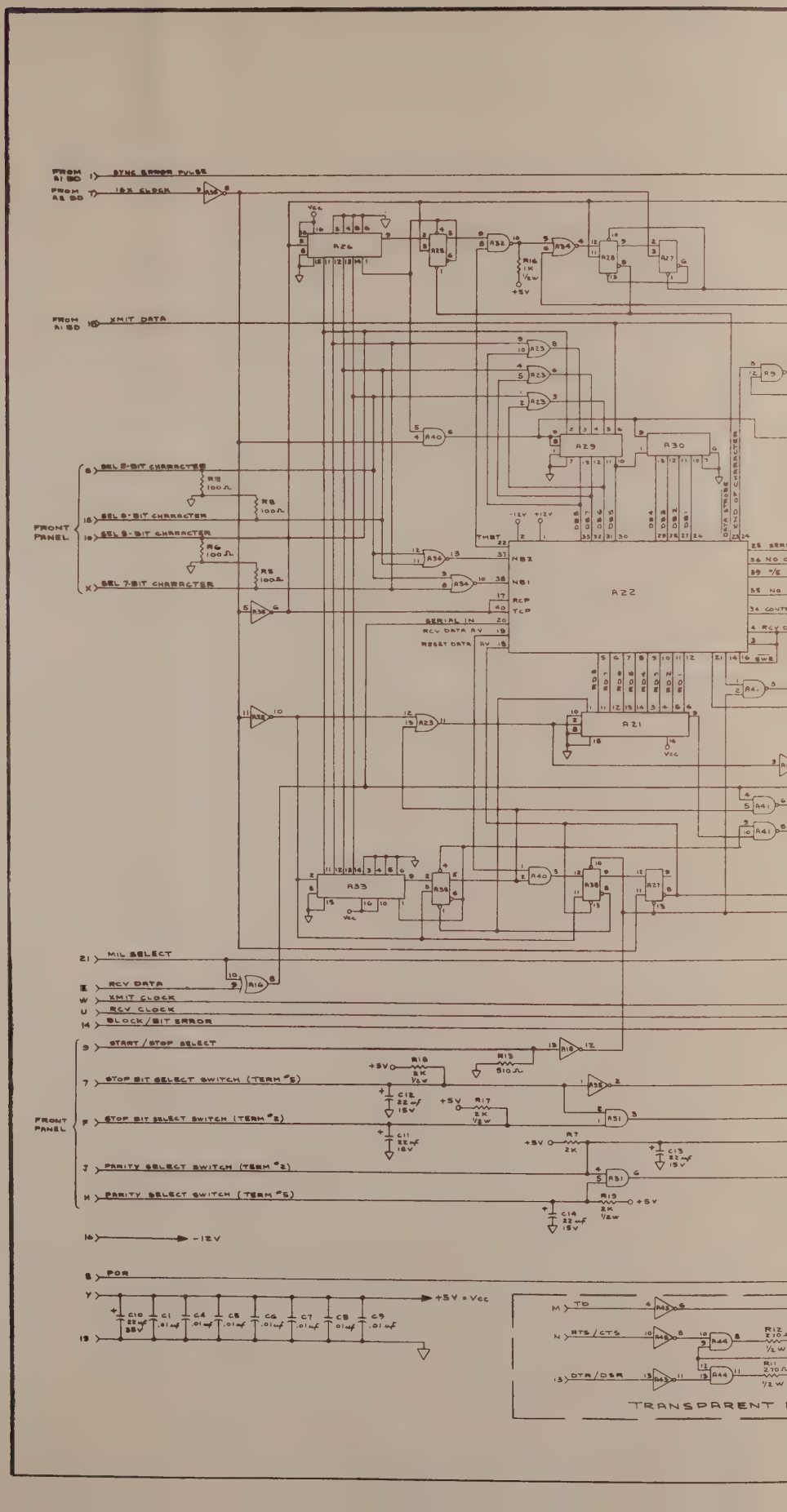
SHEET 1 OF 3 REV.

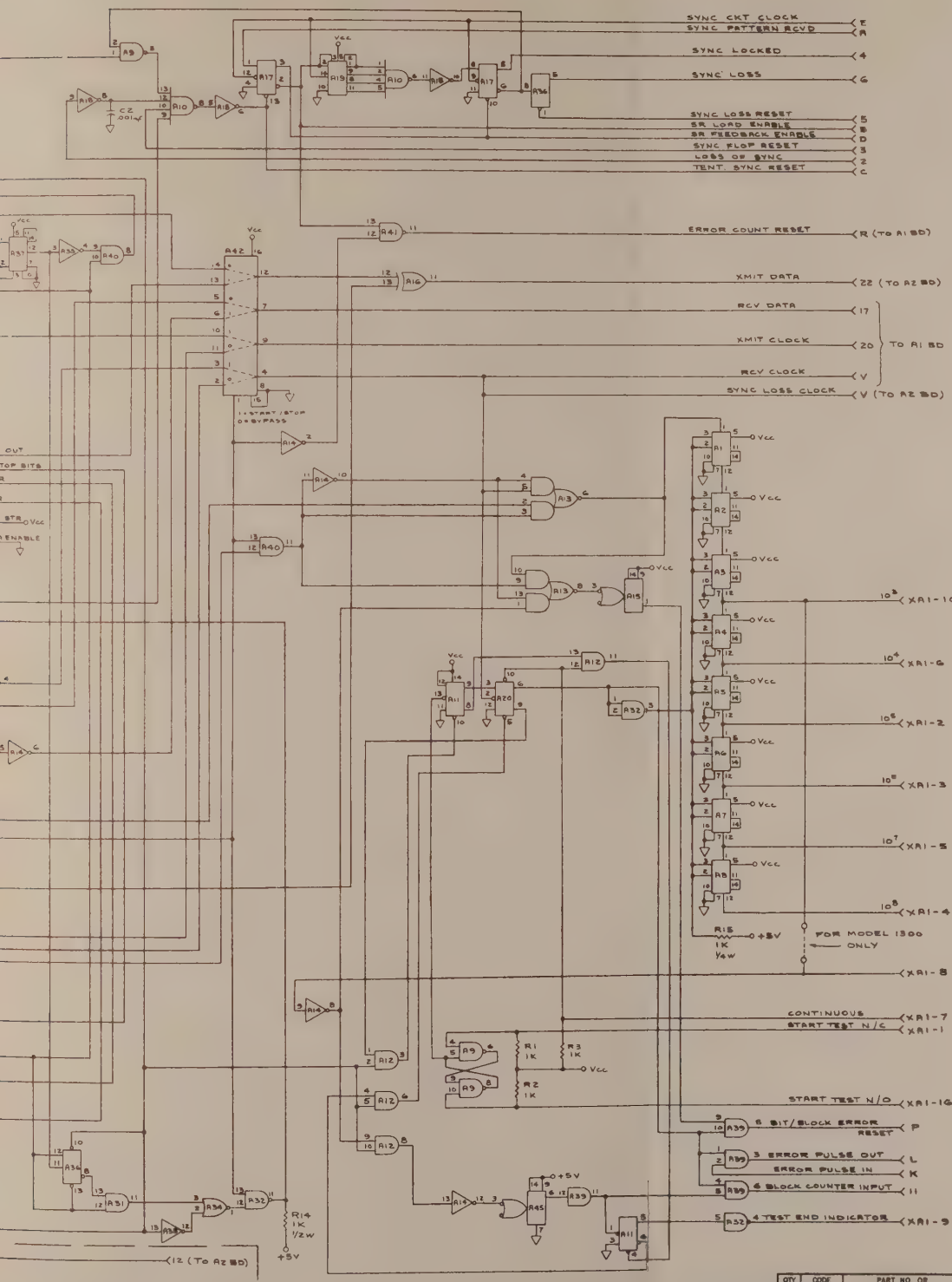
TITLE:
START/STOP OPTION
(A3 BOARD)

LTR	REVISION DESCRIPTION	DATE	APPD
Q	Retyped without Change	4/21/75	N.P.
R	REVISED ITEM Q1, C4-C9 & C10-C14 PER ECO 114-75	9-26-75	JS
S	ADDED 1200 TO SERIES NO, DELETE SHT 4 PER ECO 19-76	3-3-76	

LTR	REVISION DESCRIPTION	DATE	APPD

UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 WATT COMPOSITION, STYLE RC07
ALL CAPACITORS ARE CERAMIC, STYLE CK05


FROM A1 BD
SYNC ERROR PULSE
FROM A2 BD
16X CLOCK
XMIT DATA
FRONT PANEL
SEL 8-BIT CHARACTER
SEL 8-BIT CHARACTER
SEL 8-BIT CHARACTER
SEL 7-BIT CHARACTER
R11 100Ω
R8 100Ω
R6 100Ω
R5 100Ω
A22
A26
A27
A28
A29
A30
A31
A32
A33
A34
A35
A36
A38
A40
A41
SERIAL IN
RCV DATA AV
RESET DATA AV
MIL SELECT
RCV DATA
XMIT CLOCK
RCV CLOCK
BLOCK/BIT ERROR
START/STOP SELECT
STOP BIT SELECT SWITCH (TERM "5")
STOP BIT SELECT SWITCH (TERM "2")
PARITY SELECT SWITCH (TERM "2")
PARITY SELECT SWITCH (TERM "5")
-12V
POR
+5V = Vcc
TD
RTS/CTS
DTR/DSR
TRANSPARENT



F0-3

QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL

NEXT ASSY | USED ON
APPLICATION

CORTA NO.

DR T. GRANT 4-22-75
CHK J. Forlenza 5-5-75
APPD

APPROVED
BY DIRECTION OF

INTERNATIONAL DATA SCIENCES, INC. PROVIDENCE RHODE ISLAND

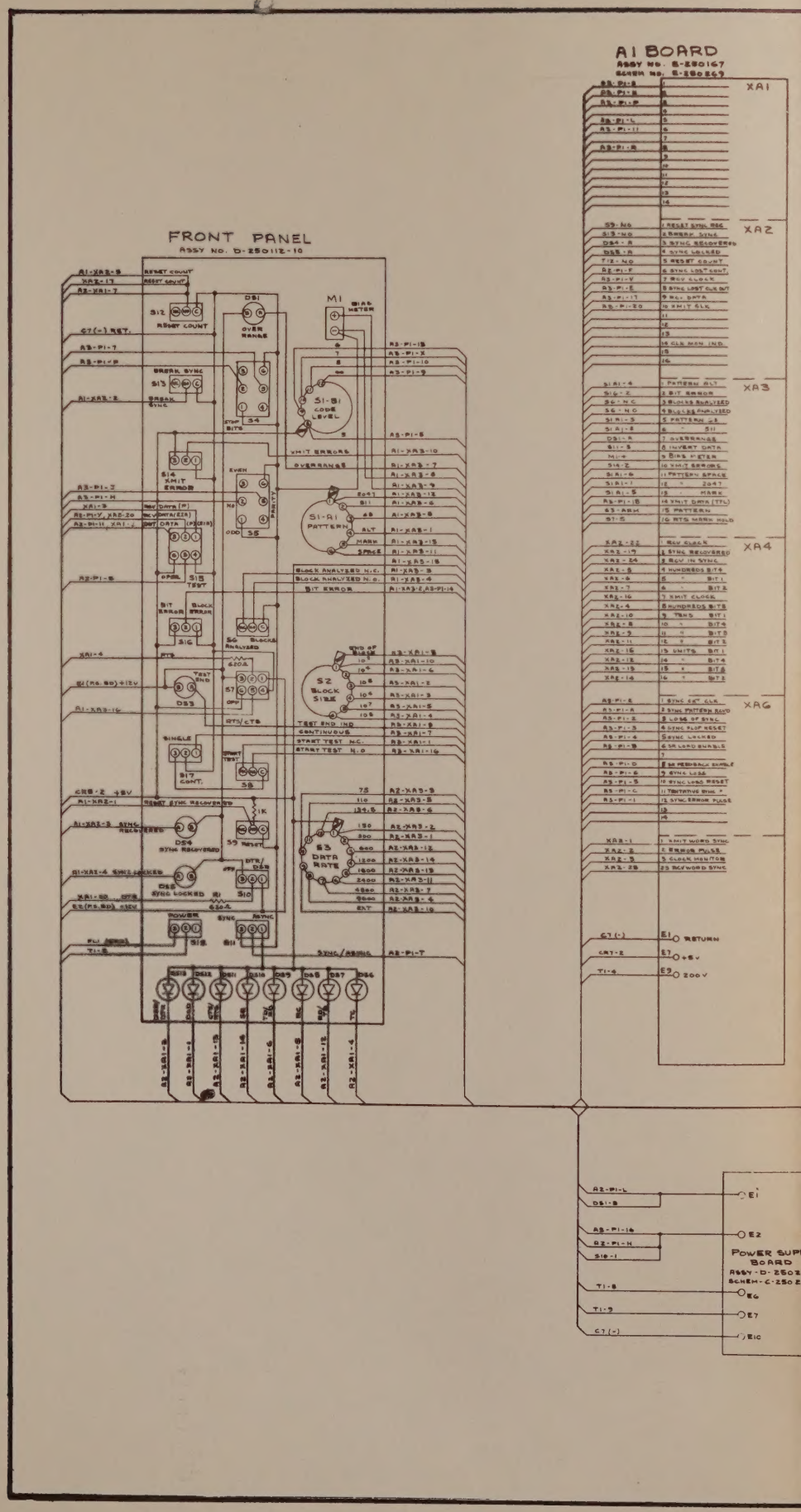
DRAWING TITLE MODEL 1310 SCHEMATIC START/STOP-A3 BD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
E	50972	250274	B

SCALE ~ SHEET 1 OF 1

PL E-250176 MODEL 1300/1310 START/STOP OPTION (A3 BOARD) SH 2

REF. DES/ ITEM NO.	QTY	PART NO.	VALUE	DESCRIPTION	VENDOR	REMARKS	CODE
		E-250176		Assembly		Printed Wiring Board	
1	1	E-250177		Detail		" "	
A1,A2,A3,A4 A5,A6,7,8,37	9	SN7490N			Texas Instru.	Delete A,4,A5, A6,A7,A8 for 1300	
A9, A41	2	MC849P			Motorola		
A10	1	SN7420N			Texas Instru.		
A11	1	MC853P			Motorola		
A12,A31,A39, A40,A44	5	MC1807P			"	A44-Use for Transp. mode only	
A13	1	SN7451N			Texas Instru.		
A14,A18,A35	3	SN7404N			" "		
A15, A45	2	MC851P			Motorola		
A16	1	SN7486N			Texas Instru.		
A17	1	SN74107N			" "		
A19	1	SN7493N			" "		
A20	1	MC845P			Motorola	Delete for 1300	
A21,A26,A33	3	SN74165N			Texas Instru.		
A22	1	AY-5-1012/TR1402A			Gen. Instru.		
A23	1	SN7432N			Texas Instru.		
A27,A28,A36 A38	4	SN7474N			" "		


A1 BOARD
ASSY NO. E-250167
SCHEM NO. E-250269
XA1
XA2
XA3
XA4
XA5
FRONT PANEL
ASSY NO. D-250112-10
M1
BIAS METER
S1-B1 CODE LEVEL
S1-A1 PATTERN
S2 BLOCK SIZE
S3 DATA RATE
POWER SUPPLY BOARD
ASSY-D-250
SCHEM-C-250
RETURN
+5V
200V

A2 BOARD

ASSY NO. E-250180
SCHEM NO. E-250270

XA1

DS12	1 DCD LED
DS13	2 DSR LED
	3
DS6	4 TD(XMIT DATA) LED
DS5	5 RD(REC DATA) LED
DS9	6 TD(XMIT DATA) LED
S13-NO	7 LED LAMP TEST
XA1-9	8 DCD
XA1-6	9 DSR
XA1-21	10 SB
XA1-5	11 CTS
DS7	12 RD(REC DATA) LED
DS11	13 CTS LED
DS10	14 SB LED
	15
	16

XA2 (XMIT)

	1
	2
	3 3600/110
	4 7200/134.5
	5 9600
	6
	7 4800
	8 150
	9 300
	10 1200
	11 75
	12 600
	13 1800
	14 2400

XA3 (RCV)

S3-2	1 300
S3-1	2 150
S3-10	3 75
S3-9	4 9600
S3-11	5 3600/110
S3-12	6 7200/134.5
S3-7	7 4800
	8
	9
S3-3	10 EXT
S3-6	11 2400
S3-5	12 600
S3-8	13 1800
S3-4	14 1200

P1

C7(-)	1 -8V RET
A2-P1-10, CR7-2	2 +8V
	3
	4
	5
	6 48V CLOCK IN
A2-P1-D	7 XMIT TIME IN
	8 CURRENT DSR
	9 CURRENT SG
A2-P1-19, A2-P1-E	10 CURRENT REC LOOP
S18-3	11 XMIT DATA(MARK/SPACE)
A2-P1-7	12 16V CLOCK
	13 CURRENT CTS
A2-P1-4	14 REC CLOCK
A2-P1-W	15 XMIT CLOCK
A2-P1-B	16 REC DATA
XA1-24	17 XMIT TIMING
A2-P1-23	18 XMIT DATA(TTL)
A2-P1-10	19 DATA A OR B SEL
	20 REC DATA DTE/TTL
	21 XMIT CLK DTE/TTL
	22 REC CLK DTE/TTL
	A +3 CONTROL
	B
A2-P1-V	C SYNC LOST CLM IN
A2-P1-T	D ASR CLK OUT
A1-XA2-8	E SYNC LOST CLK OUT
A1-XA2-9	F SYNC LOST CONT
E8 (P.S BD)	H -15 V
	J XMIT DATA(S)
	K RTS(S)
S1 (P.S BD)	L +15 V
	M XMIT DATA(P)(EIA)
	N RTS(P)
	P DUAL DATA RATE(P)
	R DUAL DATA RATE(S)
S18-5	S TEST
S11-2	T SYNC/ASYNC CONT
XA1-15	U XMIT CLK (EIA)
	V XMIT CLK (TTL)
	W REC CLK (TTL)
XA1-17	X REC CLK (EIA)
S18-2 XA2-20	Y REC DATA (EIA)
	Z REC DATA(TTL)

A3 BOARD

ASSY NO. E-250176
SCHEM NO. E-250154

XA1

SB-NC	1 START TEST N.C
S2-3	2 BLOCK S SE 10[3]
S2-4	3 " " 10[2]
S2-6	4 " " 10[1]
S2-5	5 10[0]
S2-2	6 10[4]
S17-1	7 CONTINUOUS
S2-ARM	8 END OF BLOCK
DS5-R	9 TEST END IND
S2-1	10 BLOCK SIZE 10[5]
	11 RTS/CTS IND
	12 DTR/DSR IND
	13 LAMP TEST
	14
	15
SB-NO	16 START TEST N.O

P1

A1-XA6-12	SYNC ERR-M PULSE
A1-XA6-3	[illegible]
A1-XA6-4	3 SYNC FLIP RESET
A1-XA6-5	4 SYNC LOCATE
A1-XA6-10	5 SYNC LOSS RESET
A1-XA6-9	6 SYNC LD
S4-5	7 STRIP BIT STROBE
A1-XA1-1	8 P.I.N.
S1 S1-12	9 CODE LEVEL 8C
S1 S1-11	CODE LEVEL 8
A1-XB1-6	11 B DIV CTR INPUT
	12 TD
	13 DIV/2 IN
S16-2	14 BLOCK ST ERROR
S1 S1-9	15 CODE LEVEL 5
A2 (P.S BD)	16 -12V
A1-XA2-9	17 RLY DRIVE
A1-XA2-14	18 XMIT DATA
A3-P1-21, C7(-)	19 RETURN
A1-XA2-13	20 XMIT CLK
A3-P1-19	21 INVERT DATA
A2-P1-18	22 XMIT DATA(TTL)
A1-XA6-2	ASYNC PATTERN RCVD
A1-XA6-6	B SR LOAD ENABLE
A1-XA6-11	C TENTATIVE SYNC RESET
A1-XA6-8	D SR FEEDBACK ENABLE
A1-XA6-1	E SYNC CHT CLOCK
S4-2	F STRIP BIT SHIFTER 2
S5-7	H PARITY SHIFTER 8
S6-5	J PARITY SHIFTER 8
A1-XA1-2	K ERROR PULSE IN
A1-XA1-8	L EPROM PULSE OUT
	M TRANSMIT DATA
	N RTS/CTS
A1-XA1-3	P S.T.E.ALL ERROR RESET
A1-XB1-8	R ERR-REC'D RESET
S1 S1-8	S CODE LEVEL 5
A2-P1-12	T SYN CLOCK
A2-P1-14	U P.I.N.
A1-XA2-7, A2-P1-[illegible]	V REC SYNC DETECT
A2-P1-15	W SYNC CLK
S1 S1-10	X CODE LEVEL 7
C28-2	Y +5V
A2-P1-16	Z REC DATA

REAR PANEL

ASSY NO. C-250132-1

XA1 DATA CONN. (TO DCE)

XA3-1, J1-LUG	1 CHASSIS GRD
XA3-2, XA2-B	A XMIT DATA(M)(EIA)
XA3-3, A2-E	B REC DATA(P)
XA3-5, S7, A2-N	C RTS(P)
XA3-4, A2-XA1-11	D CTS
XA3-20, A2-XA1-9	E DSR
C7(-)	F SIGNAL GRD
A2-XB1-8	H DCD
	J
	K
	L
	M
	N
A2-P1-U	P XMIT CLOCK
	R
A2-P1-R	S REC CLOCK
	T
XA3-W, J1-LUG (SHIELD)	U CTR
A2-XA1-10	V SB
	W
	X
A2-P1-17	Y XMIT TIMING
	Z

XA2 OPTION CONN.

A1 BD-1	1 XMIT SPD SYNC
A1 BD-2	2 ERROR PULSE
A1 BD-3	3 CLOCK MONITOR
A1-XA4-8	4 8 HUNDRED
A1-XB4-4	5 4
A1-XB4-8	6
A1-XB4-6	7 2 "
A1-XA4-10	8 4 TENS
A1-XA4-11	9 8 TENS
A1-XA4-9	10 1 TENS
A1-XA4-12	11 2 TENS
A1-XA4-14	12 4 UNITS
A1-XA4-15	13 8 UNITS
A1-XA4-13	14 2 UNITS
A1-XA4-5	15 1 UNIT
A1-XA4-7	16 XMIT CLOCK
S12-NO	17 RESET COUNT
XA1-2	18 XMIT DATA
A1-XA4-2	19 SYNC RECOVERED
S15-2	20 REC DATA
C7(-)	21 SIGNAL GRD
A1-XA4-1	22 REC CLOCK
A1 BD-23	23 REC WORD SYNC
A1-XA4-3	24 REC IN SYNC
J1-LUG	25 CHASSIS GRD

XA3 DATA CONN. (TO DTE)

J1-LUG	1 CHASSIS GRD
XA1-3	2 XMIT DATA
XA1-2	3 REC DATA
XA1-5	4 RTS
XA1-4	5 CTS
XA1-20	6 DSR
C7(-)	7 SIG GRD
	8
	9
	10
	11
	12
	13
	14
	15
	16
	17
	18
	19
XA1-6	20 DTR
	21
	22
	23
	24
	25

FO-4

QTY REQD	CODE IDENT NO.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
FRACTIONS ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
1 PLACE DECIMALS ±
MATERIAL:

CONTR NO.

DR T. GRANT 2-19-75
CHK'D [illegible] 4-3-75
APPD
APPROVED [illegible]
BY DIRECTION OF

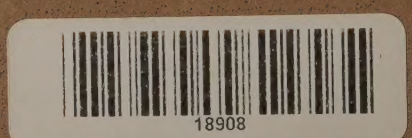
INTERNATIONAL DATA SCIENCES, INC. PROVIDENCE RHODE ISLAND

DRAWING TITLE MODEL 1310 INTERCONNECTION SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
E	50572	250268	C

SCALE ~ SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	



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